



**HIGHER
EDUCATION
PROGRAM**

2005-06

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Mentor Graphics Corporation Higher Education Program

1. Introduction

Welcome to the Higher Education Program's product catalog for 2005-06. Inside you will find details on the Mentor Graphics® products that are available to universities and colleges for the coming year. **I urge you to read all the sections of this brochure so you are aware of any changes that may affect your class or research program.**

We are pleased to add several new products and options to the available software for the coming year. Notable additions include ModelSim® System C simulation, the Precision® Physical Synthesis tool for speed critical FPGAs, Calibre® XL providing inductance extraction capabilities to Calibre xRC™, the PADS® PCB design tool suite, and the HyperLynx Signal Integrity tools for high-speed PCB analysis.

We have made one significant change for the coming year to the way that you select and order the software. Instead of selecting individual products from a checklist, you will be selecting by product package. You will then receive licenses and media for all products in that category. This ensures that you receive the maximum benefit for each package's support charge. Furthermore, it ensures that you receive a desired product and all its optional components immediately, without the need to request changes to your configuration mid-term.

The majority of products remain within the original high-level product packages; however it has been necessary to move some products, and the PCB Design category has been split into three separate packages based on each of the high-level product lines (Expedition™, PADS and Board Station®). **Please carefully study the product packages for 2005-06 to see which categories you need to order.**

As with all years, Mentor Graphics makes strategic decisions that necessitate removing some products from the catalog of available software. **Please study carefully the Product Changes section to see if and how any discontinuations affect you.**

Thank you once again for your continued support, and we hope you have a productive year as a member of Mentor Graphics Higher Education Program.

Sincerely,



Ian Burgess
Development Manager
Mentor Graphics Higher Education Program

2. How to Order Software

If you are applying for membership of Mentor Graphics Higher Education Program, or are renewing your membership for the coming year, you will need to select and order the various products you need to use for your class work and projects.

The process for prospective new members and existing members is slightly different, so please make sure you follow the appropriate set of instructions.

Applying and renewing your membership is via the online [Applications and Renewals](#) page of our website.

Please ensure that you follow the instructions carefully.

Renewing Applications

If you are returning to the Program for the following year, select the button *"I am an existing member of the Higher Education Program and I am renewing my support"*.

You will need to provide your Mentor Graphics site ID during the renewal process.

New Applications

If you are applying for membership of the Program, select *"I am not a member of the Higher Education Program, and I am applying for the first time"*.

In both cases be sure to provide complete and detailed answers to the Course/Project Information and Curriculum sections (Steps 3 and 4). This will help expedite the approval process.

3. Higher Education Product Packages 2005-06

For the year 2005-06 Mentor Graphics products available through the Higher Education Program are divided into six product packages. Table 1 shows these packages and their corresponding support prices.

Package	Description	Main Product Components	US Support Price
1	IC Nanometer Design	Eldo [®] , ADVance MS [™] , and CommLib [™] ICstudio [™] , Design Architect [®] -IC, IC Station [®] , Calibre physical verification Calibre xRC extraction	\$500
2	Design, Verification & Test	ModelSim simulation and verification FPGA Advantage [®] Precision Synthesis, Leonardo Spectrum [™] Design For Test Seamless [®] Co-Verification SystemVision [™] system modeling Logical Cable [™]	\$500
3a	PCB – Expedition	Expedition Design Capture Expedition Pinnacle Layout DxDesigner [™] I/O Designer [™] FPGA Integration Tau [®] Timing Analysis Fablink [™] XE, Fablink XE Pro HyperLynx, HyperLynx GHz Quiet [™] Expert	\$200
3b	PCB – PADS	PADS Logic PADS Layout, PADS Autorouter PADS HyperLynx, PADS HyperLynx GHz	\$500
3c	PCB – Board Station	Board Architect [™] , Design Architect [®] Board Station, Hybrid Station [®] MCM Station [®] , TeamPCB [™] RE Autorouter, RE High-Speed Tau Timing Analysis Idea Station [®] , QuickSim [™] , Accusim [®] , Continuum [™]	\$200
4	Classic IC Design	GDT [®] family Lsim [™] family MicroPlan [™] , MicroRoute [™]	\$500

Table 1 – Mentor Graphics Higher Education Program Packages, 2005-06

Full details on all products included within each package are provided beginning in Section 4.

When you order your Higher Education Program software you will select by package, and you will receive licenses and media for **all products included in that package**.

International Support Pricing

Canada and Europe

Support prices for Canada and Europe are as follows –

Package	Description	Canada Support Price	Europe Support Price
1	IC Nanometer Design	CAN \$625	EUR 525
2	Design, Verification & Test	CAN \$625	EUR 525
3a	PCB – Expedition	CAN \$250	EUR 225
3b	PCB – PADS	CAN \$625	EUR 525
3c	PCB – Board Station	CAN \$250	EUR 225
4	Classic IC Design	CAN \$625	EUR 525

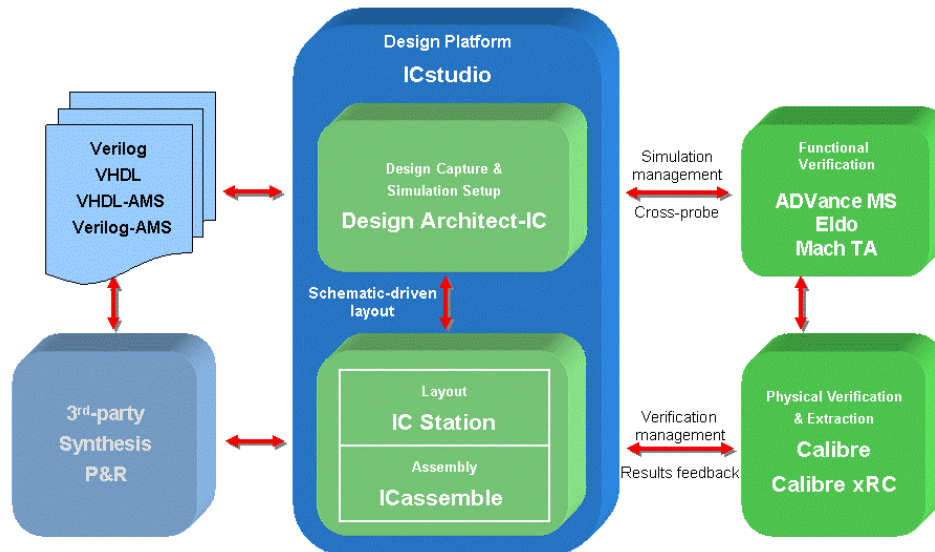
Table 2 – Higher Education Program Support Prices, Canada and Europe

Other Regions

To obtain pricing in other regions please contact your regional Higher Education Program representative (see Section 15).

4. Package 1 - IC Nanometer Design

Mentor Graphics' IC Nanometer Design package provides a complete environment for the design, capture, layout and verification of **analog, digital and mixed-signal integrated circuits**.



IC Nanometer Design Flow and Products

Package 1 includes **all products** that incorporate the IC Nanometer Design platform.

- **ICstudio** – a comprehensive and integrated solution for the creation and layout of IC's
- **Design Architect-IC** - a powerful tool for schematic capture, netlisting, simulation setup and results viewing.
- **IC Station** - provides the physical layout component of the Mentor Graphics full custom IC design flow. This suite includes application bundles for editing, schematic-driven layout, and top-level floor planning/routing.
- **ICassemble** - a robust set of features for floor planning, top-level assembly and interactive routing.
- **ADVance MS and ADVance MS RF**– a language-neutral, mixed-signal simulator that enables top-down design and bottom-up verification of multi-million gate analog/mixed-signal Soc designs.
- **Eldo and Eldo RF** – an analog simulator offering numerous simulation and modeling options that deliver high-performance and high-speed simulation with the accuracy required by the user.
- **Mach TA™** – Mach TA is a circuit simulator for Timing Analysis.
- **Calibre** – The industry standard platform for physical verification, offering Superior performance and capacity for both flat and hierarchical algorithms.
- **Calibre xRC** – Accurate transistor-level, gate-level and hierarchical parasitic extraction

Detailed Products Listing for Package 1 – IC Nanometer Design

ANALOG-MIXED SIGNAL IC SIMULATION		Available Platforms				Description
		SUN	HP	LNK	WXP	
Eldo Analog Design Stn SW	130009	x	X	x	-	A complete Analog Design environment with the Eldo kernel simulator
Eldo Kernel Ap SW	130001				-	
AMS Waveform Processor	130006				-	
Mach TA Ap SW	207920	x	X	x	-	
AMS Waveform Processor Ap SW	130006	x	X	x		Fast, accurate, high capacity, transistor-level circuit simulation for timing and power analysis Graphical postprocessor providing waveform viewing of analog and mixed-signal simulation results.
ADMS Dual Lang plus RF Stn SW	207874	x	X	x	-	The industry's first mixed –signal and RF simulation environment that brings together VHDL-AMS, Verilog-AMS, mixed-signal standard HDL and SPICE in a single environment.
ADVance MS Ap SW	205000				-	
ADVance MS Verilog Digital Op SW	207525				-	
Verilog A Op SW	207271				-	
Eldo RF Op SW	204979	x	X	x	-	
ADMS Dual Lang Mach Stn SW	207875	x	X	x		The industry's first mixed –signal simulation environment that brings together VHDL-AMS, Verilog-AMS, mixed-signal standard HDL and SPICE in a single environment.
ADVance MS Ap SW	205000					
ADVance MS Verilog Digital Op SW	207525					
Verilog A Op SW	207271					
Mach TA Ap SW	207920	x	X	x		
Eldo for HyperLynx Op SW	221154	x	X	x	-	Analog transistor level simulator
ADVance MS RF Op SW	212235	x	X	x	-	RF Analysis capability for ADVance MS
CommLib Op SW	210690	x	X	x	-	A collection of behavioral language simulation templates for telecommunications applications: Use with Accusim and Eldo RF
ADVance CommLib	210689	x	X	x	-	Telecommunications library in ADMS binary
ADVance Design Toolbox Op SW	223101	x	X	x	-	Characterization and scripting toolbox for Eldo

IC-FLOW		Available Platforms				Description
		SUN	HP	LNK	WXP	
DA-IC Viewerless Ap SW	217713	x	X	x	-	Schematic capture, netlisting, and simulation setup, integrated within the analog/mixed signal design flow.
Design Architect-IC DDP Ap SW	216571	x	X	x	-	
ICgraph Basic Ap SW	063084	x	X	x		Schematic Driven Layout and polygon editing
ICgraph SDL Ap SW	034641	x	X	x		
IC Station SDL Bnd SW	212040	x	X	x	-	Hierarchical, schematic- and netlist-driven layout environment to create IC layouts based on information from a logic source, plus ready-to-use parameterized device generators for digital and analog layout design.
ICassemble Op SW	210433	x	X	x		
Hotplot Bundle Ap SW	212041	x	X	x	-	Optimized for IC design printing and plotting – produces the most popular and efficient printer-ready formats, directly from DA-IC and IC Station SDL.
IC EDIF200 Sch Reader Bnd SW	221494	x	X	x	-	EDIF Interfaces for IC Flow
IC EDIF300/400 Sch Read Bnd SW	221495	x	X	x	-	
IC EDIF200 Sch Writer Stn SW	221496	x	X	x	-	
IC EDIF300/400 Sch Write Stn SW	221497	x	X	x	-	
IC EDIF200 Netlist Read Stn SW	221498	x	X	x	-	
IC EDIF300/400 Netlist Read Stn SW	221499	x	X	x	-	
IC EDIF300/400 Netlist Write Stn SW	221500	x	X	x	-	

ASIC / IC - Place & Route						
AutoCells Ap SW	044110	x	X	x	-	
Back Annotation Op SW	054743	x	X	x	-	
Clock Tree Op SW	054744	x	X	x	-	
Timing Driven Layout	054745	x	X	x	-	
Falcon Framework	030000	x	X	x	-	Pre-requisite infrastructure for IC Flow
Falcon Framework	051663	x	X	x	-	
Nutcracker NT Emulation	211539	x	X	x		
HP HP-GL Filter	054804	x	X	x		
HP HP-GL/2 Filter	054805	x	X	x		
Postscript Filter	054806	x	X	x		
Schematic Generator	065769	x	X	x	-	

<u>PHYSICAL VERIFICATION AND EXTRACTION</u>		Available Platforms				Description
		SUN	HP	LNX	WXP	
Calibre DFM Op SW	220523	x	X	x		Calibre DFM manages and prioritizes thousands of recommended rules errors and allows designers to analyze and modify areas of concern
Calibre DRC Ap SW	061498	x	X	x		The industry standard for design rule checking
Calibre DRC-H Op SW	061499	x	X	x		
Calibre Interactive Ap SW	210230	x	X	x		
Calibre RVE/QDB-H Ap SW	210570	x	X	x		The Calibre sub-wavelength resolution enhancement tools are the first complete physical verification and manufacturing solution
Calibre TDopc Op SW	211565	x	X	x		
Calibre PRINTimage Op SW	204414	x	X	x		
Calibre OPCsbar Op SW	211566	x	X	x		
Calibre OPCpro Op SW	204413	x	X	x		
Calibre MT-OPCpro Op SW	205564	x	X	x		
Calibre PSMgate Op SW	204415	x	X	x		
Calibre WORKbench Ap SW	204416	x	X	x		
Calibre LITHOview Ap SW	207041	x	X	x		Calibre MDP allows for seamless continuation of the data manipulations required for resolution enhancements techniques
Calibre MDPview Ap SW	210899	x	X	x		
Calibre MDPmerge Op SW	220547	x	X	x		
Calibre FRACTUREm Op SW	209427	x	X	x		
Calibre FRACTUREj Op SW	211030	x	X	x		
Calibre FRACTUREt Op SW	212329	x	x	x		Industry standard physical verification tool for layout versus schematic
Calibre LVS Ap SW	061501	x	x	x		
Calibre LVS-H Op SW	061401	x	x	x		
Calibre MT-2nd CPU Op SW	205003	x	x	x		Calibre DESIGNrev offers fast loading and visualization of multi-gigabyte GDSII layout data
Calibre DESIGNrev Ap SW	210681	x	x	x		
Calibre xRC Ap SW	210228	x	x	x		Hierarchical parasitic extraction tool that delivers accurate mixed level parasitic data for comprehensive and accurate analysis and simulation.
Calibre XL	221191	x	x	x		Inductance Extraction
xCalibrate Ap SW	067851	x	x	x		
Time-it Op SW	223155	X	X	X		Digital Delay Calculator for Calibre xRC, ADVance MS and ModelSim
ICrules Op SW	034689	x	x	x		
ICtrace Op SW	034691	x	x	x		

5. Package 2 – Design, Verification and Test

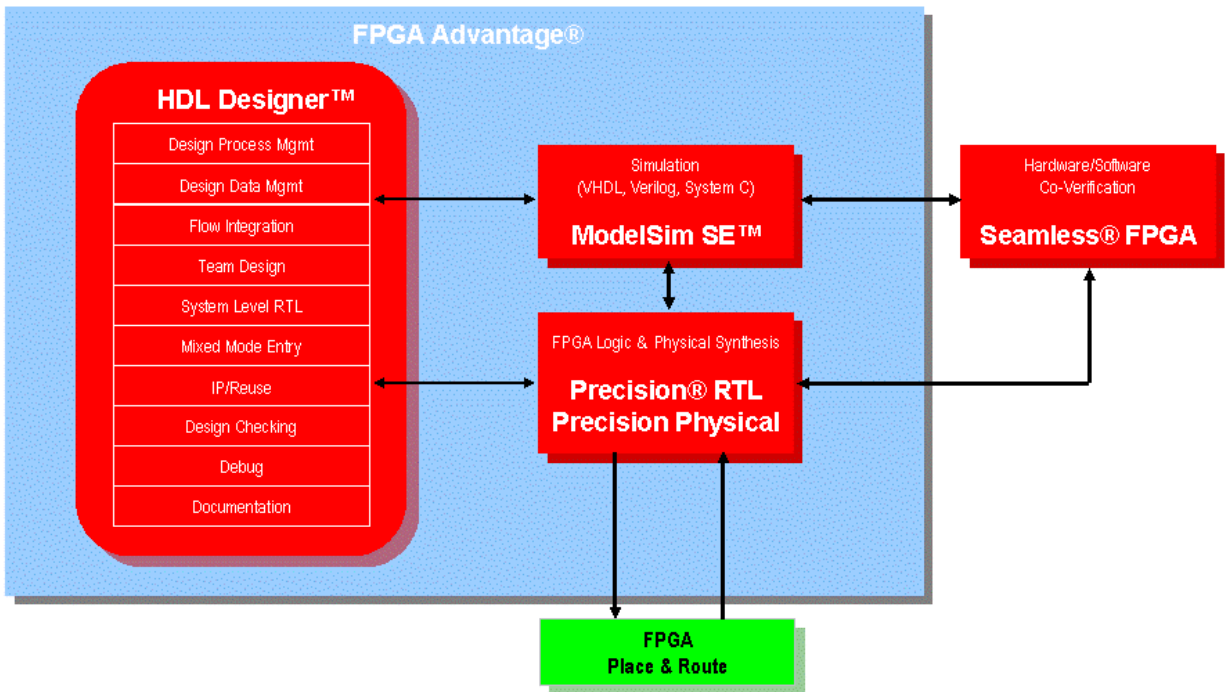
The Design, Verification and Test package provides complete solutions for HDL Design, Verification, Synthesis and Test of ASICs and FPGAs.

The products in this category comprise

- FPGA Design and Verification – A complete solution comprising HDL design, simulation, hardware-software co-verification and leading FPGA logic and physical synthesis.
- ASIC Design and Verification – A complete solution comprising HDL design, simulation, co-verification, synthesis, design-for-test and formal verification.
- Design-for-Test – A complete technology-leading solution for testability analysis, scan, boundary scan and memory test synthesis, and automatic test pattern generation.
- Hardware-Software Co-Verification – The industry's leading solution for verification of hardware and software.
- System Modeling – A complete environment for creation and verification of mixed-signal and multi-language systems, prevalent in automotive electrical systems, control systems and mechatronic systems.

FPGA Design and Verification

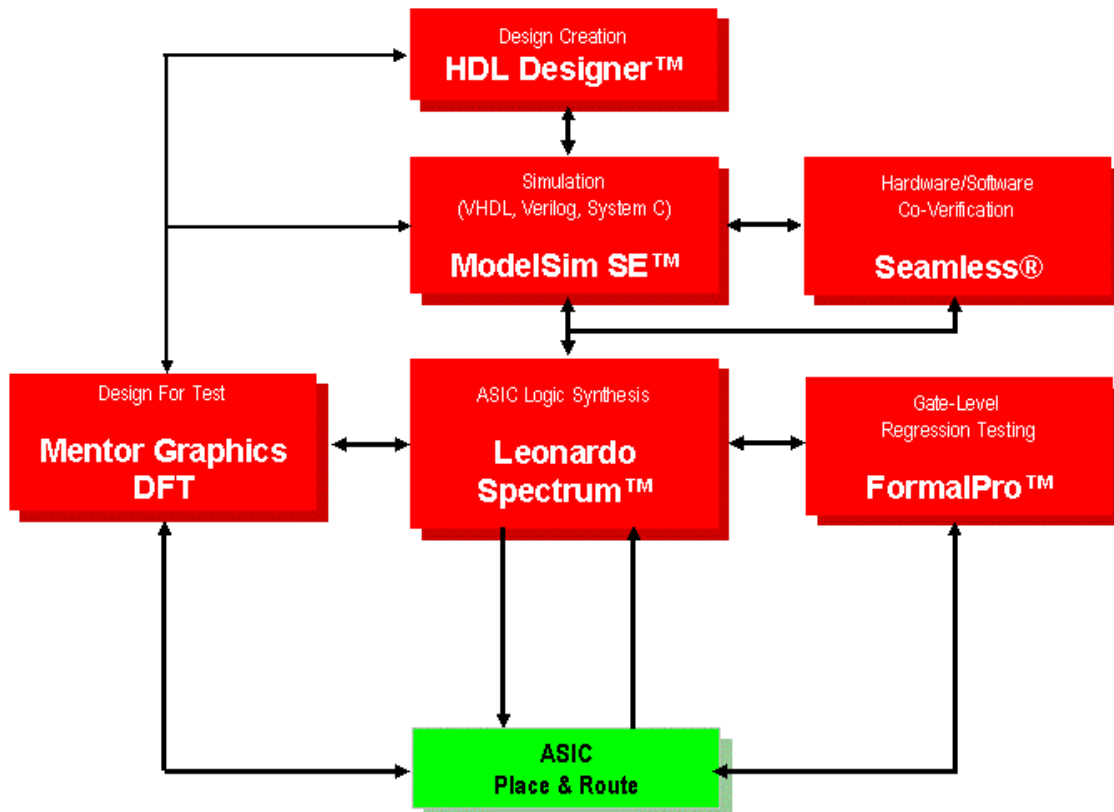
Mentor Graphics supports a complete flow for the design and verification of complex FPGAs and field programmable SOCs.



- **HDL Designer™** – A graphical HDL design environment that enables scalable RTL design, spanning FPGAs to multimillion gate ASICs. HDL Designer creates and manages complex Verilog, VHDL, and mixed-language ASIC and FPGA designs.
- **ModelSim SE™** – The industry’s most widely used verification environment. ModelSim’s single kernel architecture supports all the industry’s standard languages including **VHDL, Verilog and SystemC**.
- **Precision Synthesis** – Delivers outstanding quality of results for FPGA synthesis from VHDL and Verilog 2001.
- **Precision Physical Synthesis** – An integrated RTL and physical FPGA synthesis solution, built on a single data model, simultaneously optimizes gate and interconnect delay.
- **Seamless FPGA** – Verification of hardware and software in an embedded system, Seamless FPGA provides a single button, automated set up for FPGA verification.

ASIC Design and Verification

Mentor Graphics provides a number of best-in-class solutions for the design and verification of complex ASICs and SOCs.

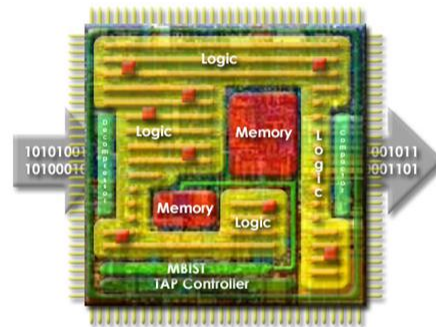


- **HDL Designer** – A graphical HDL design environment that enables scalable RTL design, spanning FPGAs to multimillion gate ASICs. HDL Designer creates and manages complex Verilog, VHDL, and mixed-language ASIC and FPGA designs
- **ModelSim SE** – The industry’s most widely used verification environment. ModelSim’s single kernel architecture supports all the industry’s standard languages including VHDL, Verilog and SystemC.
- **Leonardo Spectrum** – A push-button easy-to-use for solution for designing PLDs, FPGAs and ASICs, in VHDL or Verilog.
- **Design for Test** - Mentor Graphics’ Design-for-Test products provide a complete solution for achieving high test quality, low test cost for the whole chip.
- **FormalPro™** – A high-capacity equivalence checking solution for gate-level regression testing of designs from small to multi-million gate designs.
- **Seamless**– Verification of hardware and software in an embedded system.

Design-for-Test

Mentor Graphics' Design-for-Test products provide a complete solution for achieving high test quality, low test cost for the whole chip.

- ✓ **FastScan**
 - Automatic test pattern generation
 - All fault models
- ✓ **MacroTest**
 - Non-intrusive memory test
- ✓ **MBISTArchitect**
 - Memory Built-in Self-Test
- ✓ **DFTAdvisor**
 - Full scan insertion
- ✓ **DFTInsight**
 - Graphical DFT debugging
- ✓ **BSDArchitect**
 - Boundary scan



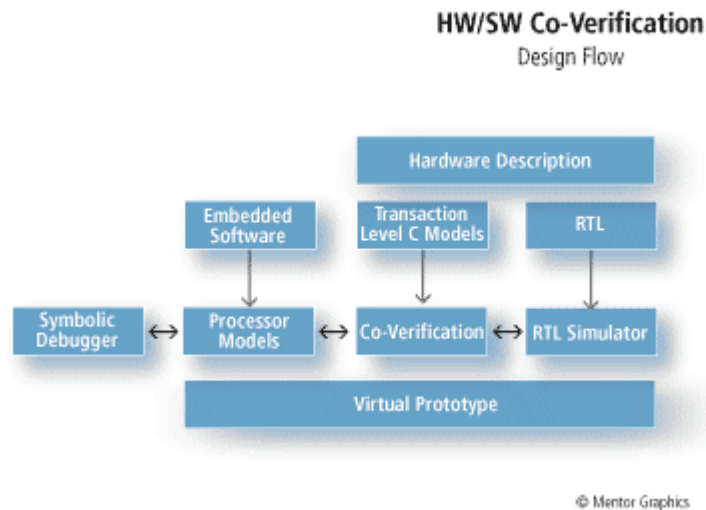
Design-for-Test Products

The DFT product family includes:

- **FastScan™** – The industry leading automatic test pattern generation (ATPG) tool.
- **DFTAdvisor™** – A comprehensive test synthesis and testability analysis tool.
- **DFTInsight** – A DFT graphical debugging environment.
- **FlexTest™**– an ATPG and fault simulation solution for non- or partial scan designs.
- **BSDArchitect™** – A solution for automating boundary scan generation.
- **MBISTArchitect™** – A comprehensive solution for achieving high quality memory built-in self-test (BIST).

Hardware/Software Co-Verification

Mentor Graphics' Seamless Co-Verification Environment provides for the verification of both hardware and software in an embedded system. Seamless allows for a virtual prototype instead of having to build a physical prototype. Early debug reduces risk of having to re-design the system.

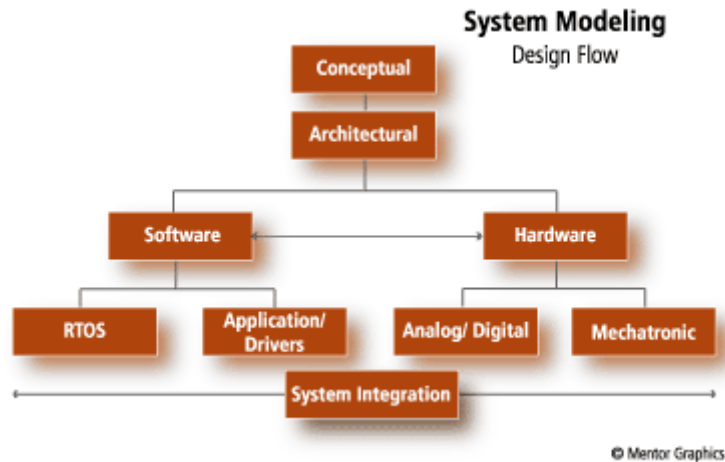


Seamless is available as two products

- **Seamless** - Co-verification environment that detects and isolates hardware/software interface errors.
- **Seamless FPGA** - Co-verification environment that detects and isolates hardware/software interface errors for Platform FPGAs. Seamless FPGA provides a single button, automated Seamless setup, and includes the PowerPC 405 Processor Support Package for the Xilinx Virtex-II technology.

System Modeling

Mentor Graphics System Modeling category provides a complete environment to create, simulate and analyze mixed-signal and multi-language systems.



System Modeling Design Flow

Product Package 2 includes SystemVision that incorporates the System Modeling platform.

- **SystemVision** – a mixed-signal modeling and simulation environment using the power of VHDL-AMS to verify your control and mechatronic systems.
- **SystemVision** is targeted at the following applications.

Automotive Electrical Systems, addressing challenges such as increased vehicle mechatronic content, dual voltage system architecture design, function design and analysis and communication systems.

Control Systems, such as system concept feasibility, digital/analog subsystem partitioning, hardware/software/firmware partitioning, subsystem IO specification and dynamic system interactions not found at the subsystem level.

Mechatronic Systems Design technology challenges such as mixed-technology systemic interactions, device sizing and component rating and algorithm testing with "software in the loop" capabilities.

Detailed Products Listing for Package 2 – Design, Verification and Test

HDL DESIGN AND VERIFICATION		Available Platforms				Description
		SUN	HP	LNX	WXP	
HDL Designer Ap SW	207964	x	X	x	x	Creates and manages complex VHDL, Verilog and Mixed-language ASIC and FPGA designs
DesignAnalyst Ap SW	222316	x	X	x	x	HDL Checker for design errors in RTL designs
ModelSim SE MixedHDL Ap SW	205146	x	X	x	x	Industry leading tri-lingual (VHDL, Verilog and SystemC) simulator
SystemC Op SW	219261	x	X	x	x	
Precision RTL Synthesis Ap SW	211639	x	X	x	x	Integrated high performance RTL and physical FPGA synthesis solution, simultaneously optimizes gate and interconnect delay
Precision Phys Synth FPGA Ap SW	216109	x	X	x	x	
Leo Spectrum Lev 3-VHDL FPGA Ap SW	204431	x	X		x	Push button synthesis tool for VHDL and Verilog synthesis
Leo Spectrum Lev 3-VLOG FPGA Ap SW	204432	x	X		x	
Spectrum Lev 3 ASIC-VHDL Ap SW	204437	x	X		x	
Spectrum Lev 3 ASIC-VLOG Ap SW	204436	x	X		x	
Leonardo Insight Op SW	222470	x	X		x	
XLIB Creator Ap SW	204439	x	X		x	
FormalPro V8 Ap SW	204610	x	X	x	-	High capacity equivalence checker for ASICs & IC's

DESIGN FOR TEST		Available Platforms				Description
		SUN	HP	LNX	WXP	
MBISTArchitect Ap SW	061484	x	X	x	-	Automates the creation of built-in self-test structures to ASICs/ICs that contain memories.
MBIST Flex Op SW	207095	x	X	x	-	
BSDArchitect V8 Ap SW	205561	x	X	x	-	Automatic boundary scan synthesis & verification for ASIC/IC designs.
DFTAdvisor Ap SW	051569	x	X	x	-	Provides testability analysis, comprehensive DFT rule checking and test synthesis of full and partial-scan designs.
DFTInsight Op SW	059201	x	X	x	-	
FastScan ATPG Ap SW	043879	x	X	x	-	Industry's premier automatic test pattern generation tool, creates high-quality tests for ASICs and IC's using full or structured partial scan.
FastScan CPA Op SW	057135	x	X	x	-	
FastScan MacroTest Op SW	202287	x	X	x	-	
FlexTest ATPG Ap SW	043880	x	X	x	-	Test pattern generation for optimal test coverage for non-scan, partial-scan or full-scan designs
ASICVector Interfaces Op SW	051449	x	X	x	-	Simulation and tester formatting of ATPG patterns

SOC VERIFICATION		Available Platforms				Description
		SUN	HP	LNx	WXP	
Platform Express Ap SW	209723	x		x	-	Design creation, configuration & verification for platform based SOCs
Seamless CVE Kernel Ap SW	204591	x		x		Delivers high power, high validity co - verification for all of today's embedded processors, reducing the risk of integration errors, and improving time -to-market.
Seamless for VIIPro Bndl SW (Seamless FPGA)	212985	x		x	x	
ARM1136 PSP Op SW	217528	x		x		ARM Processor Support Packages for Seamless CVE
AMBA7tdmi PSP Op SW	203991	x		x		
ARM7tdmi PSP Op SW	067922	x		x		
ARM740t PSP Op SW	204718	x		x		
ARM 7 & 9 Composite PSP Op SW	217351	x		x		
ARM9tdmi PSP Op SW	203990	x		x		
ARM920t PSP Op SW	203988	x		x		
ARM9e PSP Op SW	205116	x		x		
ARM9EJ PSP Op SW	209399	x		x		
ARM925 PSP Op SW	206373	x		x		
ARM926ej PSP Op SW	209463	x		x		
ARM940T PSP Op SW	202556	x		x		
ARM946 PSP Op SW	205117	x		x		
ARM966 PSP Op SW	205118	x		x		
ARM1026 PSP Op SW	217527	x		x		
ARM Graphical DebuggerPSP Op SW	206111	x		x		
MIPS 4kc PSP Op SW	203670	x		x		MIPS Processor Support Packages for Seamless CVE
MIPS 5kc PSP Op SW	203669	x		x		
MIPS 20KC PSP Op SW	210713	x		x		
MIPS 24K PSP Op SW	220723	x		x		

SYSTEM MODELING		Available Platforms				Description
		SUN	HP	LNx	WXP	
SystemVision Pro Ap SW	214315				x	A virtual lab for creating and analyzing, digital, analog and mixed-signal systems
SystemVision Devices Op SW	220903				x	
SystemVision Booster Op SW	220683				x	
DxDatabook	215721				x	Wiring connectivity editor for cabling & harness design
Logical Cable V8 Op SW	034623	x	x		x	
Falcon Framework	030000	x	x		x	
Design Architect	034617	x	x		x	
Nutcracker NT Emulation	211539	x	x		x	

6. Packages 3a, 3b, 3c – PCB Design and Analysis

Mentor Graphics is the market leader in PCB design, implementation and analysis. Our integrated solutions support a complete flow for design definition with schematics and HDL, FPGA integration for reduced design cycles, an integrated layout and routing environment and powerful signal integrity analysis tools.

For the Higher Education Program Mentor Graphics has two new product offerings in the area of printed circuit board design. These are –

- **Expedition**– the most powerful solution targeted at the mid-sized to large organization or for the systems design group with pervasive use of leading edge PCB or high speed technologies.
- **PADS**– a complete PCB design solution combining schematic definition with powerful layout and simulation tools.

Included in each of these product lines is **HyperLynx**, Mentor's powerful signal integrity analysis suite. The HyperLynx suite of tools can be used in virtually any design flow to help eliminate signal integrity, crosstalk, and EMC problems early, allowing you to "get it right the first time." These simulation tools come ready to use with unprecedented ease of use, delivering high speed analysis to every engineer's desktop.

Mentor Graphics also continues to enhance and support the **Board Station** product line. Board Station is available to select members of the Higher Education Program.

For more information on the PCB Product Packages and the changes to the PCB products for the Higher Education Program, please view the following sections:

- **Which PCB Products to Use?**
- **Changes to the Higher Education Program PCB Offerings**
- **PCB Frequently Asked Questions**

Which PCB Products to Use?

The category of PCB products you choose should be determined by the type of course or project that you are running at your establishment.

- **Expedition** is a complete enterprise solution for the design, layout and analysis of PCB systems, and is typically used by medium to large companies for the implementation of telecommunication infrastructure, aerospace, and complex and high-speed consumer applications. **Expedition is the most powerful of Mentor Graphics' PCB product lines and is most appropriate for courses that intend to teach PCB design and analysis as a core skill or trade, such as technical colleges, community colleges, trade schools or training centers.**
- **PADS** is an easy to use PCB design product targeted at small companies carrying out simple designs. While still powerful, it has fewer capabilities than Expedition. **PADS would be most appropriate as an easy to learn tool where PCB design is not being taught as a core skill, such as university electronics degree projects** incorporating many electronic design disciplines.

Profile	Recommended Product Package
Technical College, Community College or Trade School teaching PCB Design as a core competence, such as a certificate or Associates Degree	Expedition
University requiring a PCB package as part of a large project, where PCB implementation is required, but not as a core competence	PADS
Projects requiring highly concurrent design of FPGA and PCB	Expedition

Table 3 – Recommended PCB Packages based on College Curriculum

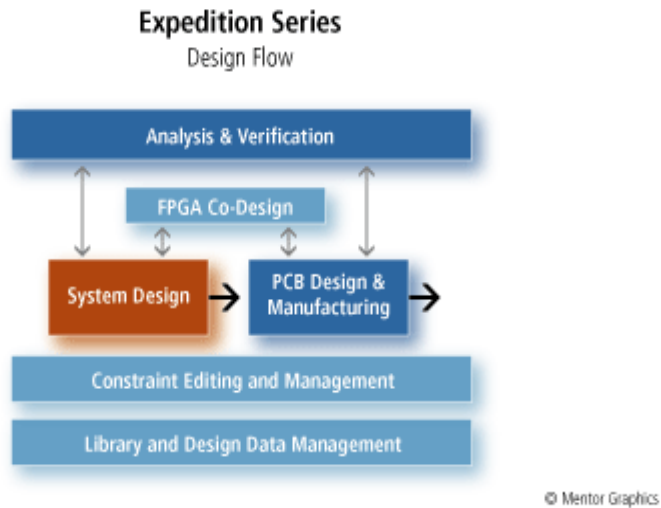
Changes to the Higher Education Program PCB Offerings

From 2005-6, Mentor's PCB product lines will be offered in separate complete packages, providing a complete solution for each of the product lines. If you are an existing member of the Higher Education Program this is a change from previous years where the products were grouped into a single category.

Please read carefully the package descriptions below to determine which package or packages you require. Please also study the frequently asked questions section for further guidance.

As your product requirements may span multiple packages, we have priced the Expedition and Board Station packages at \$200 each. This ensures that if you are an existing program member requiring both Board Station and Expedition packages, you will pay no more than previous years.

7. Package 3a – PCB Expedition



The Expedition Series flow is tailored for the mid-sized to large enterprise organization or for the systems design group with pervasive use of leading edge PCB or high speed technologies. This tightly integrated systems design solution is composed of the industry's most advanced design and analysis functionality in an environment of constraint, library and design data management.

- Most advanced placement and routing technology for high design productivity, fast time-to-market, and performance optimized products.
- High-speed pre and post-layout analysis for classical MHz routes and multi-gigabit serial interconnects.
- Design capability for leading PCB technologies such as HDI/microvia, embedded components, flex and rigid –flex, and for high pin-count/performance IC packages.
- Tight integration with FPGA design solutions for reduced design cycle time and optimized system performance.
- Common constraint editing and management system feeds all tools in the flow for one-time, easy-to-use entry.
- Patented concurrent team design technology reduces layout design time by 40-70%.

Package Highlights

For the Higher Education Program, the Expedition Series package includes the following –

- **Design Capture and System Design** - Expedition Design Capture, DxDesigner Series Products, Analog Designer
- **Timing Analysis** – Tau
- **PCB Layout** – Expedition Pinnacle, Team PCB, IS_Analyzer™, IS_Synthesizer™
- **FPGA Integration** – I/O Designer
- **Manufacturing** – CAM Output Manager, Fablink XE, Fablink XE Pro
- **Signal Integrity Analysis** – HyperLynx, HyperLynx GHz, Quiet Expert

Detailed Products Listing for Package 3a – PCB Expedition

Bolded X = Recommended Platform for this package

3A - PCB EXPEDITION BND SW	224321	Available Platforms				Description
		SUN	HP	LNx	WXP	
ICX Waveform Analyzer Op SW	222191	x	X	x	x	Signal integrity analysis and analysis-driven interconnect synthesis and board-level autorouting
IS Synthesizer Ap SW	204418	x	X	x	x	
IS_Analyzer Ap SW	204422	x	X	x	x	
IS FloorPlanner Ap SW	204419	x	X	x	x	
IS Optimizer Ap SW	204420	x	X	x	x	
IS MultiBoard Op SW	204417	x	X	x	x	
TAU Ap SW	221331	x	X	x	x	Exhaustive worst case timing analysis for PCBs
Design Capture Ap SW	206052			x	x	Expedition PCB design capture with procedural interface with configuration management and tool launching.
Design Capture PI Ap SW	206068			x	x	
DesignView Ap SW	206050			x	x	
EDIF 2.0.0 Schematic I/F Ap SW	206069		X	x	x	
Expedition PCB Pinnacle Ap SW	222402			x	x	Layout, analysis, and manufacture of highly-complex PCBs based upon AutoActive™ which simplifies the design process while ensuring high quality, manufacturable results.
Expedition PCB Browser Ap SW	206079			x	x	
ePlanner Expedition Op SW	219937			x	x	Team-based PCB design for Expedition
TeamPCB - WG Op SW	215737			x	x	
Analysis Toolbox Op SW	206141			x	x	
Design for Manufacturing Op SW	206144			x	x	
High Speed Module Op SW	206145			x	x	
IDF Interface Op SW	206082			x	x	
Advanced Interconnect Op SW	206143			x	x	
DxExp Variant Manager Bndl SW	221965	x	X	x	x	Bill of Materials management tool
DxVariantManager Op SW	215723	x	X	x	x	
Variant Manager Op SW	206413	x	X	x	x	
CAM Output Manager-Admin Ap SW	209413				x	Interface to FPGA design tools allowing concurrent design of FPGA and PCB
CAM Output Manager-Client ApSW	209412				x	
I/O Designer Ap SW	219171				x	
Parts Manager Admin Ap SW	206072	x	X	x	x	Library parts management
Parts Manager Client Ap SW	206073	x	X	x	x	
Library Manager Ap SW	206071	x	X	x	x	
PCB Planner Ap SW	206059				x	Facilitates initial placement and routing of critical components and interconnect. Read-only display environment allows a design to be concurrently viewed while it is in progress.
PCB Viewer Ap SW	206060				x	
OrCad schematic Exp IF Op SW	215981				x	Analog Signal Simulation
Analog Designer Ap SW	206070				x	
Exp IFF Interface Op SW	212131				x	
Exp Design Reuse Op SW	212132				x	
Exp Basic Automation Op SW	220416				x	

DxDesigner 100 Bndl SW	215732	x	X		x	The foundation for design definition, library and data management, design reuse, component selection
DxDesigner 050 Ap SW	215734	x	X		x	
DxDataBook Op SW	215721	x	X		x	
DxPDF Op SW	215719	x	X		x	
DxDataManager Op SW	215720	x	X		x	
DxVariantManager Op SW	215723	x	X		x	
Connectivity Sprdsht Editor Op SW	218323	x	X		x	
DxLibrary Studio Op SW	215718	x	X		x	
DxRFI Op SW	217811	x	X		x	
Spice Integration Op SW	215729	x	X		x	
PC/PCB CAD Interfaces Op SW	213194				x	EMI/EMC analysis for PCBs
QUIET Expert Ap SW	220414	x	X		x	
QuietExpert Upgrade SW	220525				x	
Fablink XE Ap	220907	x	X	x	x	Multiple design panel creation and editing capabilities
Fablink XE Pro	220633	x	X	x	x	

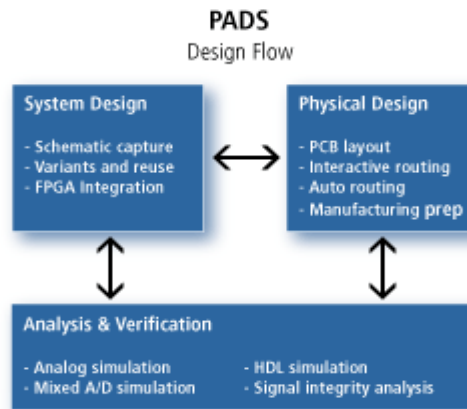
HYPERLYNX SIGNAL INTEGRITY PRODUCTS							
HyperLynx EXT Bndl SW	215735					x	Signal integrity analysis to determine the transmission line characteristics of PCBs including ringing, overshoot, undershoot and delay.
HyperLynx LineSim Ap SW	215731					x	
LineSim EMC Module Op SW	214036					x	
LineSim Crosstalk Module Op SW	214038					x	
HyperLynx BoardSim Ap SW	215730					x	
BoardSim EMC Module Op SW	214027					x	
BoardSim Crosstalk Module Op SW	214029					x	
HyperLynx GHz Bndl SW	217671					x	
HyperLynx LineSim GHz Ap SW	217663					x	
HyperLynx BoardSim GHz Ap SW	217661					x	
HL EXT SPICE Writer Mod Op SW	214212	x					Signal integrity analysis to address the needs of multi-gigabit design
HyperLynx IBIS Dev Sys Ap SW	217665					x	
BoardSim SPICE Writer Mod Op SW	214028					x	
HL Expedition I/F Op SW	214825					x	
LineSim SPICE Writer Mod Op SW	214037					x	
BoardSim EBD Writer Module Op SW	214197					x	
BoardSim Multi-Board AnlysMod Op SW	214198					x	
FlowXpert Ap SW	056401		X			x	
ProjectXpert Ap SW	056403		X			x	
XpertBuilder Ap SW	056402		X			x	
HP Hp-GL Filter	054804	x				x	A runtime, multi-user process manager . Deploy and manage the execution of established best design practices throughout your engineering organization. Track and monitor project status and progress. Project administration for WorkXpert. Create visually intuitive standardized flows to capture best design practices for reuse and improvement.
HP HP-GL/2 Filter	054805	x				x	
Postscript Filter	054806	x				x	

8. Package 3b – PADS

PADS is a complete PCB design solution combining schematic definition with powerful layout and simulation tools. It provides an integrated design environment combines ease of use with functional depth.

With PADS PCB design solutions, you will:

- Achieve a high ROI on PCB designs ranging from basic to complex.
- Improve productivity with shorter design cycles.
- Maintain design integrity with the latest analysis and simulation tools.



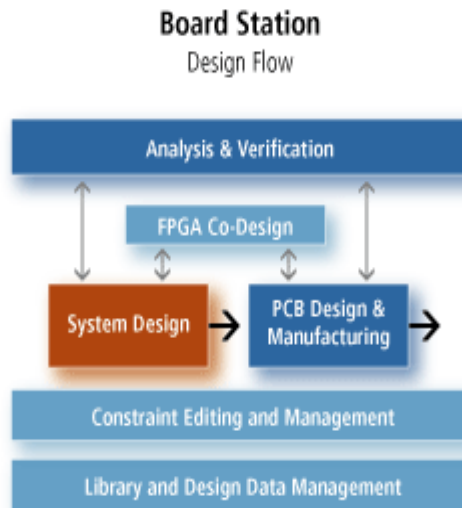
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Detailed Products Listing for Package 3b – PADS

3B - PADS		Available Platforms				Description
		SUN	HP	LNX	WXP	
PADS Logic Op SW	214735				x	PADS Schematic Capture
PADS Layout 395 Kit SW	221318				x	PADS PCB layout
PADS AutoRouter HSD Op SW	214734				x	PADS autorouting for high-speed designs
IDF Link Op SW	214747				x	Mechanical engineering interface
Adv Packaging Toolkit Op SW	214760				x	Any angle BGA routing
PADS-HL EXT Bndl SW (HyperLynx Signal Integrity Analysis)	218521				x	HyperLynx signal integrity analysis for PADS
PADS-HL GHz Bndl SW (HyperLynx GHz Signal Integrity Analysis)	218524				x	HyperLynx GHz signal integrity analysis for PADS
P DxDesigner 050 Ap SW	216653				x	Personal productivity design entry

9. Package 3c – Board Station

The Board Station family of products continues to provide loyal users with constant infusions of productivity enhancing and groundbreaking technologies. All without interrupting the massive, high-volume businesses that create the most adopted technologies and leading products that shape our world today.



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Board Station Package

For the Higher Education Program, the Board Station package includes the following –

- **Design Capture and System Design** – Board Architect, Design Architect
- **Timing Analysis** – Tau
- **PCB Layout** – Board Station, Interactive Layout, Hybrid Station, MCM Station, IS_Synthesizer, IS_Optimizer™, RF Layout, TeamPCB, RE Autorouter, RE High-Speed
- **Board Simulation** – Idea Station, QuickSim, Accusim, Continuum

Detailed Products Listing for Package 3c – Board Station

3C - BOARD STATION FAMILY PCB PRODUCTS		Available Platforms				Description
		SUN	HP	LNx	WXP	
Board Architect Stn V8 SW	062000	x	x	x	x	Advanced schematic design entry tool for the PCB design process.
Design Architect Ap SW	034617	x	x	x	x	
Board Architect Upg SW	061999	x	x	x	x	
Board Stn V8 SW	039986	x	x	x	x	A complete PCB layout package
Librarian V8 Ap SW	034638	x	x	x	x	
Fablink V8 Ap SW	034637	x	x	x	x	
Board Layout V8 Ap SW	035302	x	x	x	x	
ARTROUTER grid V8 Op SW	039994	x	x	x	x	
Hybrid Stn V8 SW	039987	x	x	x	x	Complete system for designing thick-film hybrids & PCBs
Librarian V8 Ap SW	034638	x	x	x	x	
Fablink V8 Ap SW	034637	x	x	x	x	
Board Layout V8 Ap SW	035302	x	x	x	x	
Hybrid V8 Ap SW	042839	x	x	x	x	
ARTROUTER grid V8 Op SW	039994	x	x	x	x	
MultiChipMod Dsnr Stn V8 SW	044164	x	x	x	x	Interactive design of multi-chip modules
Librarian V8 Ap SW	034638	x	x	x	x	
Fablink V8 Ap SW	034637	x	x	x	x	
Board Layout V8 Ap SW	035302	x	x	x	x	
Hybrid V8 Ap SW	042839	x	x	x	x	
High Spd Interactive V8 Op SW	044156	x	x	x	x	
Scepter FAB V8 Ap SW	063003	x	x	x	x	Bi-directional data exchange between CAD and CAM
Scepter DFF V8 Ap SW	063004	x	x	x	x	
Scepter DFA V8 Op SW	063189	x	x	x	x	
Scepter Milling&Drill V8 Op SW	063190	x	x	x	x	
Scepter Panel V8 Op SW	063191	x	x	x	x	
RE AutoRouter V8 Op SW	206644	x	x	x	x	Interactive PCB Layout Editing and routing with re-route
RE Network AutoRouter V8 Op SW	206646	x	x	x	x	
RE HighSpeed V8 Op SW	206645	x	x	x	x	
ICX Waveform Analyzer Op SW	222191	x	x	x	x	Signal integrity analysis and analysis-driven interconnect synthesis and board-level autorouting
IS Synthesizer Ap SW	204418	x	x	x	x	
IS_Analyzer Ap SW	204422	x	x	x	x	
IS FloorPlanner Ap SW	204419	x	x	x	x	
IS Optimizer Ap SW	204420	x	x	x	x	
IS MultiBoard Op SW	204417	x	x	x	x	
ICX Standard Library Op SW-SL	217757	x	x	x	x	
TAU Ap SW	221331	x	x	x	x	Exhaustive worst case timing analysis for PCBs
	215736	x	x	x	x	Team-based PCB design for Board Station
TeamPCB - EN Op SW						
ProtoView V8 Ap SW	034640	x	x	x	x	Pre-placement and analysis of PCBs
EngineerView Lite V8 Op SW	057119	x	x	x	x	
Hispeed Lite V8 Op SW	057123	x	x	x	x	High-speed interactive option for Protoview
ManufactureView V8 Ap SW	057105	x	x	x	x	View-only station for manufacturing
PCB PACKAGE V8 Ap SW	034635	x	x	x	x	Application for packaging logic functions into physical components
Interactive Layout V8 Ap SW	051637	x	x	x	x	

PCB Mechanical I/F V8 Op SW	042732	x	x	x	x	Interface to mechanical design
PTM:SITE V8 Op SW	051576	x	x	x	x	Concurrent physical test implementation
AutoTherm V8 Ap SW	034625	x	x	x	x	Board-level thermal analysis software
RF Architect V8 Op SW	067977	x	x	x	x	Extends Board Architect to RF design
RF Layout V8 Op SW	067978	x	x	x	x	Extends Board Station to RF design
RF EM Sim Interface Op SW	202131	x	x	x	x	Interface to HP Eesof

BOARD SIMULATION PRODUCTS						
Continuum QS Stn SW	203465	x	x	x	x	Mixed signal simulation using Accusim and QuickSimII
QuickSim II Kernel V8 Op SW	034656	x	x	x	x	
Accusim II Kernel V8 Op SW	051615	x	x	x	x	
QuickSim Pro V8 Op SW	059278	x	x	x	x	
Continuum Connector Op SW	203468	x	x	x	x	
<u>Accusim-HDLA Analog DsnStn SW</u>	066919	x	x	x	x	Top-down circuit design and simulation using Accusim and HDL-A
Design Architect Ap SW	034617	x	x	x	x	
SimView V8 Ap SW	035562	x	x	x	x	
Accusim II Kernel V8 Op SW	051615	x	x	x	x	
HDL-A/DEV V8 Op SW	051630	x	x	x	x	
Idea StationII SW	220391	x	x	x	x	Logic design and simulation using Design Architect and QuickSim II
Design Architect Ap SW	034617	x	x	x	x	
SimView V8 Ap SW	035562	x	x	x	x	
QuickSim II Kernel V8 Op SW	034656	x	x	x	x	
QuickCheck Runtime V8 Op SW	039055	x	x	x	x	
EDIF 300-400 Netlist Writer Op SW	218757	x	x	x	x	
EDIF 200 Netlist Writer Op SW	217333	x	x	x	x	
QuickFault II Kernal V8 Op SW	034649	x	x	x	x	
BPL-Dig Analysis V8 Op SW-SL	059834	x	x	x	x	
BPL-CAD Lib V8 Op SW-LSL10	217771	x	x	x	x	
Accuparts V8 Op SW	034657	x	x	x		
WORKFLOW PRODUCTS						Workflow management product to track design flow Project administration for WorkXpert. Graphical workflow builder
FlowXpert Ap SW	056401	x	x		x	
ProjectXpert Ap SW	056403	x	x		x	
XpertBuilder Ap SW	056402	x	x		x	
Falcon ITK V8 Ap SW	051640	x	x		x	
NETLIST READERS & WRITERS						
EDIF 200 Netlist Reader Op SW	217332	x	x	x	x	
EDIF 200 Netlist Writer Op SW	217333	x	x	x	x	
EDIF 200 Schm Reader Op SW	218751	x	x	x	x	
EDIF 200 Schm Writer Op SW	218753	x	x	x	x	
EDIF 300-400 Schm Reader Op SW	218752	x	x	x	x	
EDIF 300-400 Schm Writer Op SW	218755	x	x	x	x	
EDIF 300-400 Netlist Reader Op SW	218756	x	x	x	x	
EDIF 300-400 Netlist Writer Op SW	218757	x	x	x	x	
HDLWrite PLUS V8 Ap SW	205653	x	x	x	x	
Schematic Generator	054769	x	x	x	x	
PRE-REQUISITE SOFTWARE						
Falcon Framework V8 Ap SW	030000	x	x	x	x	
Nutcracker NT emulation Ap SW	211539	x	x	x	x	
HP Hp-GL Filter	054804	x	x	x	x	
HP HP-GL/2 Filter	054805	x	x	x	x	
Postscript Filter	054806	x	x	x	x	

PCB Products

Frequently Asked Questions

1. Why has the previous single PCB category been split into multiple packages?

Mentor Graphics markets three distinct product lines for PCB design and analysis; Expedition, Board Station and PADS (of which Expedition and Board Station have previously been available under the Higher Education Program). From this year we are separating the Expedition and Board Station products into their own self-contained packages. All the functionality included in the previous PCB category will be available in either or both of these packages (subject to the product changes detailed in Section 11). Additionally we are introducing the PADS suite in its own package.

2. Do the changes to the PCB packages result in any cost changes?

In making the changes to the PCB product packages we have taken account of the fact that some members may be using products that now span two PCB product packages instead of one. Therefore, **we have reduced the support price for each of the Expedition and Board Station packages to \$200** instead of the previous support fee of \$504 for the single category.

Therefore, if ordering the equivalent functionality, the support charge for the PCB products will actually decrease.

3. Which PCB Design package or packages should I choose?

The category of PCB products you choose should be determined by the type of course or project that you are running at your establishment.

Expedition is a complete enterprise solution for the design, layout and analysis of PCB systems, and is typically used by medium to large companies for the implementation of telecommunication infrastructure, aerospace, and complex and high-speed consumer applications. Expedition is the most powerful of Mentor Graphics' PCB product lines and is most appropriate for courses that intend to **teach PCB design and analysis as a core skill or trade, such as technical colleges, community colleges, trade schools or training centers.**

PADS is an easy to use PCB design product targeted at small companies carrying out simple designs. While still powerful, it has fewer capabilities than Expedition, and would not be appropriate for teaching PCB as a core skill. PADS would be most appropriate as an easy to learn tool where PCB design **is not being taught as a core skill, such as university electronics degree projects** incorporating many electronic design disciplines.

4. I have been using Board Station but also need access to products included in the Expedition package. How can I get access to these additional products?

You may order both Board Station and Expedition packages at your renewal.

5. Why is the support for the PADS package priced at \$500 while support for Expedition and Board Station are priced at \$200 each?

We have reduced the support fees for the Expedition and Board Station packages as a direct result of splitting one large package into two, and to ensure that the large numbers of members who use tools across both product lines will not be adversely affected. PADS is a new addition to the Higher Education Program and accordingly its support fee is set in line with the standard Higher Education Program packages.

10. Package 4 – Classic IC Design

The Classic IC Design Package is only available to existing users within the Higher Education Program.

The Classic IC Design package provides the older Mentor Graphics products used for custom IC design. The package includes –

- GDT family of products, such as GDT Developer, Datapath™, Led™ and Lsim.
- MicroPlan and Microroute family

Detailed Products Listing for Package 4 – Classic IC Design

SPECIAL INTEREST - CLASSIC IC		Available Platforms			
		SUN	HP	LNX	WXP
Datapath Ap SW	044121	x	x	x	
GDT Developer Ap SW	044111	x	x	x	
Lcore Ap SW	044112	x	x	x	
LED Layout Ap SW	059261	x	x	x	
Led Schematic Ap SW	044128	x	x	x	
Lsim Ap SW	044101	x	x	x	
Lsim Power Analyst Op SW	057163	x	x	x	
MicroPlan Ap SW	044113	x	x	x	
MicroRoute Ap SW	044020	x	x	x	

11. Product Changes from 2003-2004

There are a number of changes to the product availability within the Higher Education Program portfolio for this year. Please study these changes carefully to determine whether and how they affect you.

Product Category Changes

In addition to the changes made to the PCB design categories, the following products have been moved to new packages.

- **SystemVision** moves from Category 3 (PCB) to Package 2 (**Design, Verification and Test**).
- **Accusim HDLA Analog Design Station** and **Analog II Design Station** are moved from Category 1 (IC Nanometer Design) to Package 3c (**PCB Board Station**).
- **WorkXpert** is moved from Category 4 (Special Interest) to Packages 3a (**PCB Expedition**) and 3c (**PCB Board Station**).
- **Logical Cable** is moved from Category 4 (Special Interest) to Package 2 (**Design, Verification and Test**).

Product Deletions

The following products are no longer offered under the Higher Education Program. Where possible, Mentor makes recommendations regarding a product transition or an alternative product.

- **xCalibre®/ICextract™** – The xCalibre product (which includes the ICextract program) has been superseded by the Calibre xRC product. All the functionality previously provided by xCalibre is provided in **Calibre xRC**.
 - Customers should switch to Calibre xRC at the earliest opportunity.
 - We are no longer shipping xCalibre/ICextract licenses to Higher Education Program Members. Members are automatically receiving licenses for Calibre xRC.
 - Customers using the ASIC Design Kit (ADK) should download the latest version 3.0. This version provides full library support for Calibre xRC.
- **SimWave** – The SimWave product is no longer supported by Mentor Graphics. Simwave has been replaced by the *AMS Waveform Processor* (also known as *EZWave*). All the functionality previously provided by Simwave is provided by *AMS Waveform Processor*.
 - Customers should switch to *AMS Waveform Processor* at the earliest opportunity. Higher Education program members automatically receive licenses for the *AMS Waveform Processor*.
 - Mentor Graphics is unable to ship any further licenses for Simwave. All support for SimWave has been transferred to *AMS Waveform Processor*. As of March 15, 2005, SimWave is no longer supported.

- **GerbTool** – The GerbTool product is no longer supported by Mentor Graphics. There is no direct replacement for GerbTool, though some functionality is provided in *Fablink XE*.
 - Existing users of GerbTool may continue to receive licenses. However, licenses will not be shipped automatically, and customers must request these licenses explicitly on the renewal form. GerbTool works with the latest releases of Expedition and Board Station, but it is not supplied on the latest media. Therefore, in order to access GerbTool, you must retain an installation of Expedition WG2004.1.
 - If you are an existing GerbTool user and wish to continue to receive licenses **you must explicitly request the product using the Special Requests section of the Product Selection menu**. You should specify **GerbTool** in this area.

- **AutoCells™ Parallel Route** – The *AutoCells Parallel Route* product has been discontinued. Mentor Graphics will no longer renew support agreements for this product. For existing support contracts we will provide reasonable efforts technical support.
 - Other *AutoCells* products, such as *AutoCells*, *Back Annotation*, *Clock Tree* and *Timing Driven Layout* are unaffected and continue to be offered within the *Package 1 – IC Nanometer Design package*.
 - Existing users of *AutoCells Parallel Route* may continue to use the product. Technical support will be provided up to your next contract renewal. Beyond that date you may continue to use the product as is, but with the understanding that no support and no new updates will be provided.
 - At your next Higher Education Program renewal you will have to explicitly request that *AutoCells Parallel Route* be provided, as authorization codes for discontinued products are not supplied automatically.
 - If you are an existing *AutoCells Parallel Route* user and wish to continue to receive licenses you must explicitly request the product using the Special Requests section of the Product Selection menu. You should specify *AutoCells Parallel Route* in this area.

- **Lsim DSM™** – The *Lsim DSM* product has been discontinued. Mentor Graphics will no longer renew support agreements for this product. For existing support contracts we will provide reasonable efforts technical support.
 - Other *Lsim* products, such as *Lsim* and *Lsim Power Analyst* are unaffected and continue to be offered within *Package 4 – Special Interest: Classic IC Design package*.
 - Existing users of *Lsim DSM* may continue to use the product. Technical support will be provided up to your next contract renewal. Beyond that date you may continue to use *Lsim DSM* as is, but with the understanding that no support and no new updates will be provided.
 - At your next Higher Education Program renewal you will have to explicitly request that *Lsim DSM* be provided, as authorization codes for discontinued products are not supplied automatically.

- If you are an existing *Lsim DSM* user and wish to continue to receive licenses you must explicitly request the product using the Special Requests section of the Product Selection menu. You should specify *Lsim DSM* in this area.

- **SST Velocity[®]** – Development of *SST Velocity* has been discontinued. Mentor Graphics will no longer renew support agreements for this product. For existing support contracts we will provide reasonable efforts technical support.
 - Existing users of *SST Velocity* may continue to use the product. Technical support will be provided up to your next contract renewal. Beyond that date you may continue to use *SST Velocity* as is, but with the understanding that no support and no new updates will be provided.
 - At your next Higher Education Program renewal you will have to explicitly request that *SST Velocity* be provided, as authorization codes for discontinued products are not supplied automatically.
 - If you are an existing *SST Velocity* user and wish to continue to receive licenses you must explicitly request the product using the Special Requests section of the Product Selection menu. You should specify *SST Velocity* in this area.

- **Seamless Processor Support Packages (PSP)** – The Seamless CVE PSPs available under the Higher Education program have been updated, with some PSPs being added and others removed. For a complete list of PSPs that are available please check the detailed product portfolio for Seamless CVE within *Package 2 – Design Verification and Test* package.

- **FPGA Boardlink** – *FPGA Boardlink* has been replaced by I/O Designer. The functionality of I/O Designer contains all the functionality previously provided by *FPGA Boardlink*.
 - *FPGA Boardlink* customers selecting *Package 3a – PCB: Expedition* will automatically receive licenses for IO Designer at your next renewal.

Product Additions

The following products have been added to the Higher Education program portfolio. Upon selecting the appropriate product category, Higher Education program members will automatically receive licenses for these products at your next renewal.

Package 1: IC Nanometer Design

- Advanced Design Toolbox
- Calibre XL, Calibre MDP Merge, Calibre DFM, Calibre FRACTUREt™
- Calibre xRC

Package 2: Design, Verification and Test (formerly HDL Design)

- Precision Physical Synthesis
- Leonardo Spectrum XLIB Creator
- DesignAnalyst™
- ModelSim System C
- Seamless Virtex-II (Seamless FPGA)
- Seamless CVE Processor Support Packages (PSP) – The Seamless CVE PSPs available under the Higher Education program have been changed, with some PSPs being added and others removed. For a complete list of PSPs that are available please check the detailed product portfolio for the Design Verification and Test package.

Package 3a – PCB Expedition

- ePlanner®
- Team PCB WG (for Expedition)
- DxDesigner, DxDatabook™, DxPDF™, DxDataManager™, DxVariantManager™, Connectivity Spreadsheet Editor, DxLibraryStudio, DxRFI Option
- Spice Integration Option
- Quiet Expert
- HyperLynx (LineSim®, LineSim EMC, LineSim Crosstalk, BoardSim®, BoardSim EMC, BoardSim Crosstalk)
- HyperLynx GHz (LineSim GHz, BoardSim GHz)
- HyperLynx IBIS Development System, Multi-Board Analysis, BoardSim SPICE Writer, LineSim EXT SPICE Writer
- Fablink XE, Fablink XE Pro

Package 3b – PCB PADS

- PADS Software suite –
 - PADS Logic, PADS Layout 395, Autorouter, IDF Link
 - Advanced Packaging Toolkit
 - PADS HyperLynx, PADS HyperLynx GHz
 - PADS DxDesigner

12. ASIC Design Kit

The ASIC Design Kit (ADK) is a generic design kit providing all the requisite data, libraries, and documentation to create ASIC designs using the Mentor Graphics suite of layout, synthesis, simulation, and DFT tools. Its primary use is by universities and colleges in class work environments.

The target technologies are AMI 0.5m and 1.2m and TSMC 0.35m, 0.25m and 0.18m.

The kit provides:

- Support for schematic, HDL or mixed schematic/HDL based designs
- Synthesis support for Leonardo Spectrum
- Pre-layout timing simulations with QuickSim and ModelSim (VHDL or Verilog)
- Scan insertion support for DFTAdvisor
- Automatic test pattern generation support for FastScan or FlexTest
- Static timing analysis models for SST Velocity
- Automatic place and route of designs using IC Station
- Post-layout timing simulations with QuickSim, ModelSim (VHDL/Verilog), Mach TA, or Eldo
- Support for Design Architect-IC

The latest version of the ASIC Design Kit is ADK 3.0. This version supports all appropriate tools in the Higher Education Program packages.

For further information, and to register and download the ADK and documentation, please visit the [ASIC Design Kit Website](#).

13. Software Support

As a member of the Higher Education Program you are entitled to the same customer support services as standard Mentor Graphics customers.

Mentor Graphics' customer support is recognized for its quality and responsiveness and has been awarded the Software Technical Assistance Recognition (STAR) award for technical excellence five times.

There are many features of Mentor's customer support that you can take advantage of to assist you with installation, usage and reporting of technical issues.

[SupportNet](#) is Mentor's online support service and provides the fastest and easiest way to resolve your technical and licensing support issues, including

- **SupportNet KnowledgeBaseSM** - an intelligent online query database to access technical notes and solutions to previously addressed solutions.
- **Service Requests** - online logging of technical and licensing support requests. Online requests are handled with exactly the same priority as phone support. You can often provide more information using online requests (such as error transcripts) that help the support engineer resolve your problem faster. You may also track your service requests whether logged online or by telephone.
- **Download of Product Updates and Patches** for all Mentor Graphics products, to bring you the latest improvements in product functionality, usability and performance.
- **Telephone support** is provided via Mentor's international network of support centers.

In addition, you may also log service requests with your [local customer support center](#) by telephone.

SupportNet Registration takes only a few minutes. You require your standard contact details and your Mentor Graphics site number. Access is immediate; you will receive 72 hours access while your registration is checked and confirmed.



The only 5 time [recipient of the Software Technical Assistance Recognition \(STAR\) Award](#) in EDA for technical support excellence.



The only EDA support provider with global support center practices [certified by the Support Center Practices \(SCP\)](#)

14. Training

Mentor Graphics offers a wide range of onsite classes and Web-based events designed to help you apply our products to meet your specific needs. Our experienced instructors apply hands-on techniques that improve learning retention and on-the-job productivity. An extensive array of online courses can also be taken at anytime to accommodate even the busiest of schedules.

As part of the Higher Education Program, faculty and specified teaching staff members are eligible to attend Mentor Graphics' advertised public training classes at zero cost on a space available basis.

To view all training classes offered by Mentor Graphics, visit the [Education Services Website](#).

To Register For a Training Class:

- Visit the [Training site](#) and browse the training catalog.
- Look up the [schedule of available classes](#)
- Call 1-800-345-2308 to reserve your spot and tell them you are a member of the Higher Education Program.
- Click here to reserve and schedule [international training](#).

15. How to Contact Us

Support

For support issues, including technical questions and licensing issues, please visit [Mentor's Customer Support](#).

The Americas

North American Contact

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Additionally, Mentor Graphics partners with the Canadian Microelectronics Corporation (CMC) to donate our IC, FPGA and ASIC design tools to CMC member Universities. CMC provides end-user support and manages annual software updates to the latest revision of our tools.

Canadian Microelectronics Corporation

210A Carruthers Hall
Kingston, Ontario
CANADA K7L 3N6

PHONE: (613) 530-4666
FAX: (613) 548-8104
URL: <http://www.cmc.ca/about/program/mentor.html>

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Additionally, Mentor Graphics partners with the EUROPRACTICE Software Service to donate our EDA tools to Universities. EUROPRACTICE looks after end-user telephone support and manages annual software updates to the latest revision of our tools.

Europractice

Microelectronics Support Centre
Rutherford Appleton Laboratory
Chilton
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Oxfordshire OX11 0QX
United Kingdom
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FAX: +44 (0)1235 44 5546
EMAIL: enquiries@msc.rl.ac.uk
URL: <http://www.te.rl.ac.uk/europractice/software/mentor.html>

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