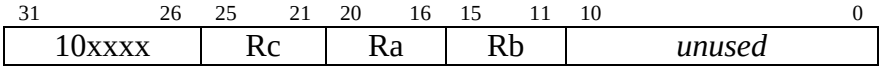
Summary of β Instruction Formats

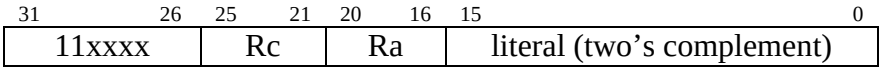
Operate Class: (*optional opcodes)



Reg[Rc] ← Reg[Ra] op Reg[Rb]

Opcodes: ADD, SUB, MUL*, DIV*
AND, OR, XOR
CMPEQ, CMPLT, CMPLE
SHL, SHR, SRA

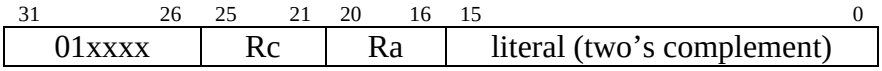
Register	Symbol	Usage
31	R31	Always zero
30	XP	Exception pointer
29	SP	Stack pointer
28	LP	Linkage pointer
27	BP	Base of frame pointer



Reg[Rc] ← Reg[Ra] op SEXT(literal)

Opcodes: ADDC, SUBC, MULC*, DIVC*
ANDC, ORC, XORC
CMPEQC, CMPLTC, CMPLEC
SHLC, SHRC, SRAC

Other:



LD: Reg[Rc] ← Mem[Reg[Ra] + SEXT(literal)]
ST: Mem[Reg[Ra] + SEXT(literal)] ← Reg[Rc]
JMP: Reg[Rc] ← PC + 4; PC ← Reg[Ra]
BEQ: Reg[Rc] ← PC + 4; if Reg[Ra] = 0 then PC ← PC + 4 + 4*SEXT(literal)
BNE: Reg[Rc] ← PC + 4; if Reg[Ra] ≠ 0 then PC ← PC + 4 + 4*SEXT(literal)
LDR: Reg[Rc] ← Mem[PC + 4 + 4*SEXT(literal)]

Opcode Table: (*optional opcodes)

5:3 \ *2:0*	*000*	*001*	*010*	*011*	*100*	*101*	*110*	*111*
000								
001								
010								
011	LD	ST		JMP		BEQ	BNE	LDR
100	ADD	SUB	MUL*	DIV*	CMPEQ	CMPLT	CMPLE	
101	AND	OR	XOR		SHL	SHR	SRA	
110	ADDC	SUBC	MULC*	DIVC*	CMPEQC	CMPLTC	CMPLEC	
111	ANDC	ORC	XORC		SHLC	SHRC	SRAC	