ROUTING 17

Key terms and concepts: Routing is usually split into **global routing** followed by **detailed routing**.

Suppose the ASIC is North America and some travelers in California need to drive from Stanford (near San Francisco) to Caltech (near Los Angeles).

The floorplanner decides that California is on the left (west) side of the ASIC and the placement tool has put Stanford in Northern California and Caltech in Southern California.

Floorplanning and placement define the roads and freeways. There are two ways to go: the coastal route (Highway 101) or the inland route (Interstate I5–usually faster).

The global router specifies the coastal route because the travelers are not in a hurry and I5 is congested (the global router knows this because it has already routed onto I5 many other travelers that are in a hurry today).

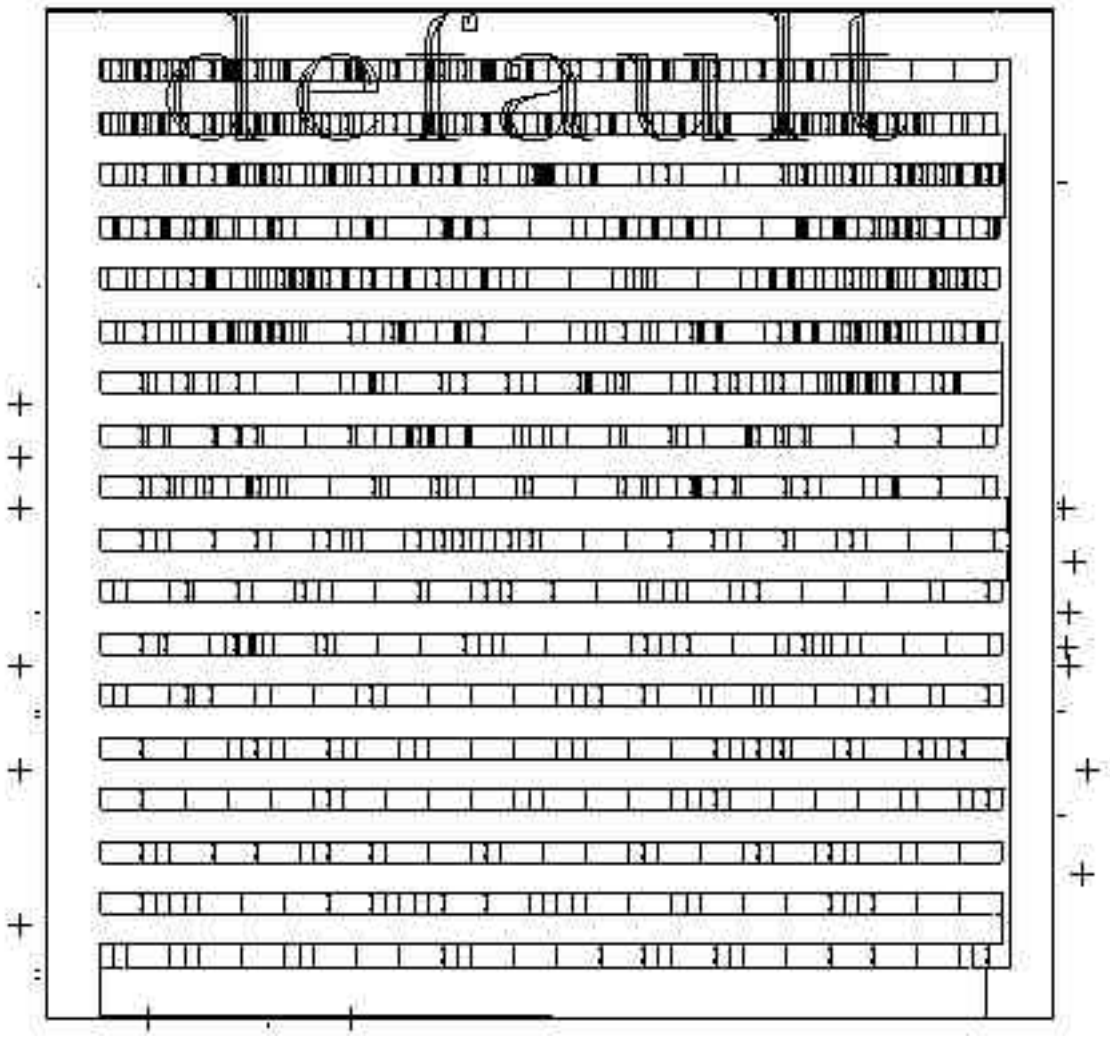
Next, the detailed router looks at a map and gives indications from Stanford onto Highway 101 south through San Jose, Monterey, and Santa Barbara to Los Angeles and then off the freeway to Caltech in Pasadena.

17.1 Global Routing

Key terms and concepts: Global routing differs slightly between CBICs, gate arrays, and FPGAs, but the principles are the same • A global router does not make any connections, it just plans them • We typically global route the whole chip (or large pieces) before detail routing • There are two types of areas to global route: inside the flexible blocks and between blocks

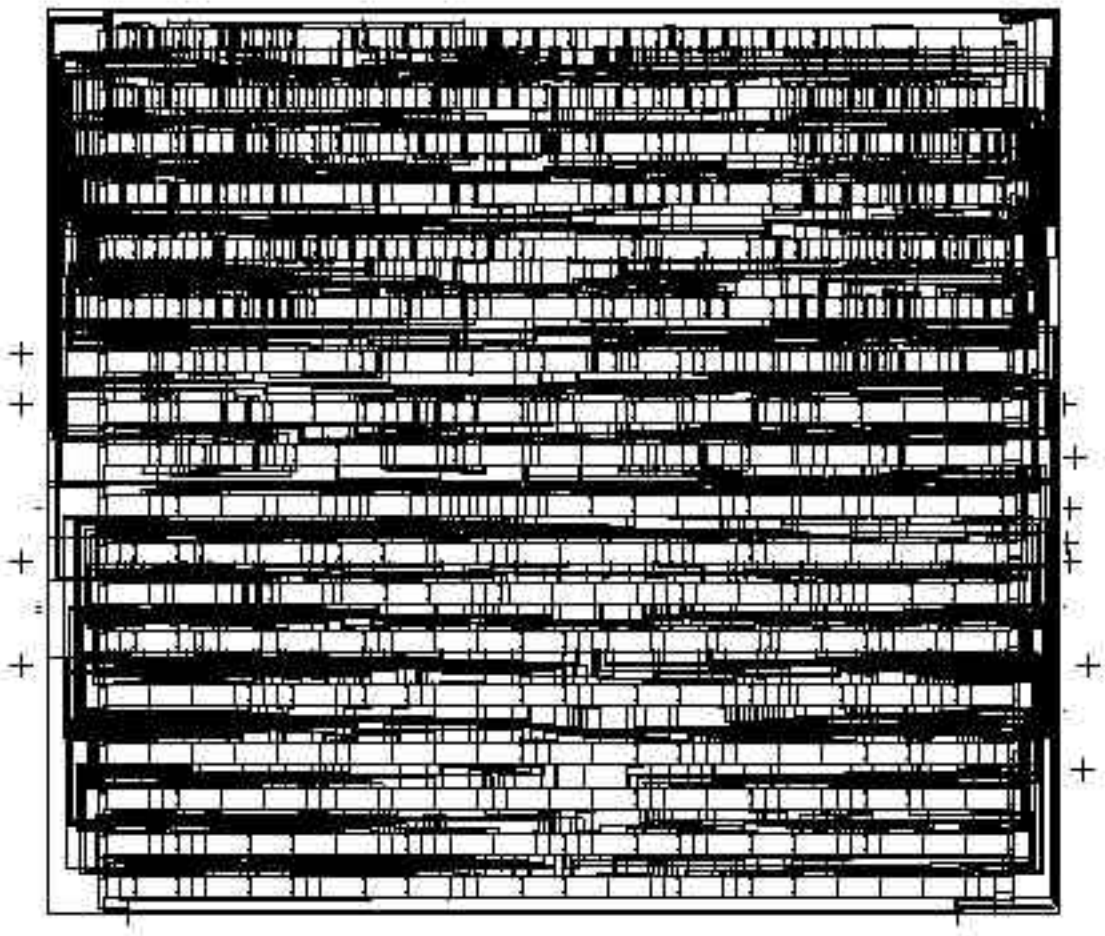
17.1.1 Goals and Objectives

Key terms and concepts: Goal: provide complete instructions to the detailed router • Objectives: Minimize the total interconnect length • Maximize the probability that the detailed router can complete the routing • Minimize the critical path delay



The core of the Viterbi decoder chip after placement.

You can see the rows of standard cells; the widest cells are the D flip-flops.



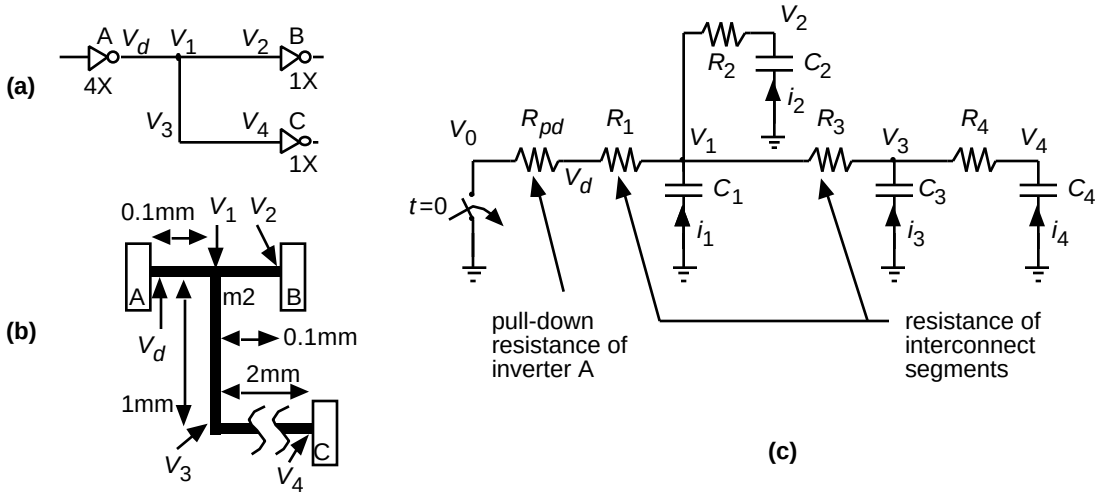
The core of the Viterbi decoder chip after the completion of global and detailed routing.

This chip uses two-level metal.

Although you cannot see the difference, m1 runs in the horizontal direction and m2 in the vertical direction.

17.1.2 Measurement of Interconnect Delay

Key terms and concepts: **lumped-delay model • lumped capacitance •** as interconnect delay becomes more important other, more complex models, are used



Measuring the delay of a net.

(a) A simple circuit with an inverter A driving a net with a fanout of two.

Voltages V_1, V_2, V_3, and V_4 are the voltages at intermediate points along the net.

(b) The layout showing the net segments (pieces of interconnect).

(c) The RC model with each segment replaced by a capacitance and resistance.

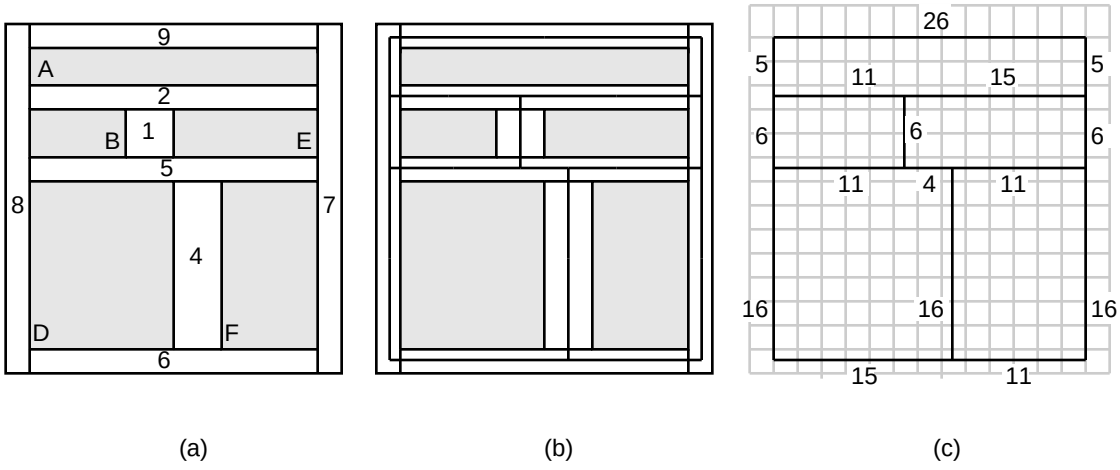
The ideal switch and pull-down resistance R_{pd} model the inverter A.

17.1.3 Global Routing Methods

Key terms and concepts: sequential routing • order-independent routing • order dependent routing • hierarchical routing (top-down or bottom-up)

17.1.4 Global Routing Between Blocks

Key terms and concepts: use of the channel-intersection graph



Global routing for a cell-based ASIC formulated as a graph problem.

(a) A cell-based ASIC with numbered channels.

(b) The channels form the edges of a graph.

(c) The channel-intersection graph. Each channel corresponds to an edge on a graph whose weight corresponds to the channel length.

17.1.5 Global Routing Inside Flexible Blocks

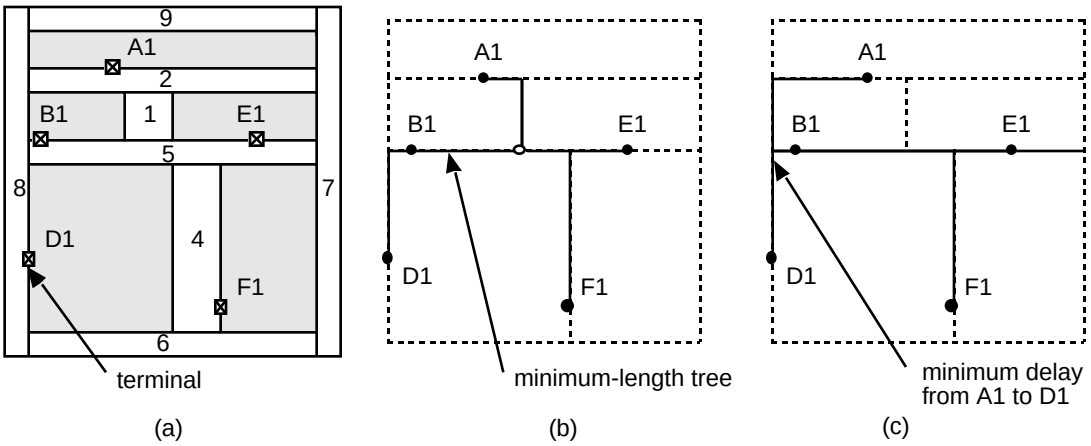
Key terms and concepts: track • landing pad • pick-up point, connector, terminal, pin, or port • area pick-up point• horizontal tracks• routing bins (or just bins, also called global routing cells or GRCs)

17.1.6 Timing-Driven Methods

Key terms and concepts: use of timing engine • path or node based

17.1.7 Back-annotation

Key terms and concepts: RC information • huge files • database problem

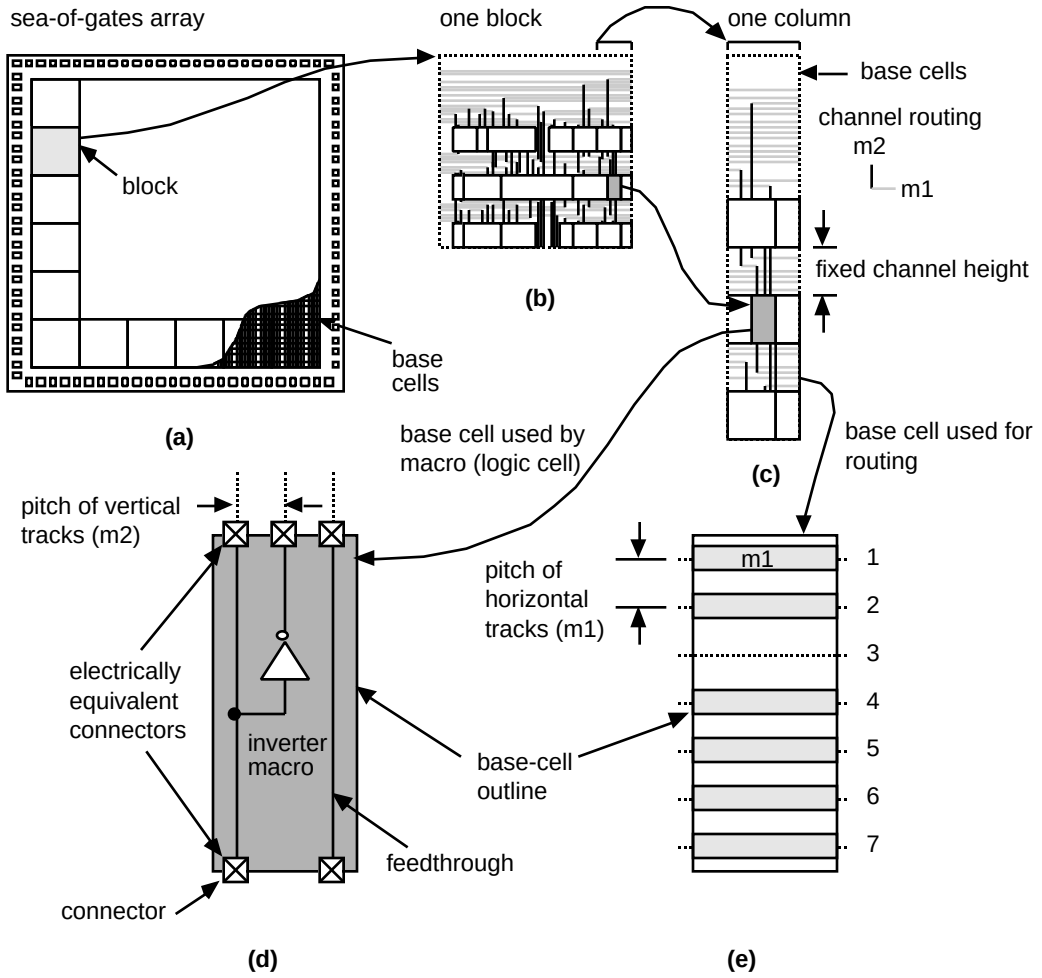


Finding paths in global routing.

(a) A cell-based ASIC showing a single net with a fanout of four (five terminals). We have to order the numbered channels to complete the interconnect path for terminals A1 through F1.

(b) The terminals are projected to the center of the nearest channel, forming a graph. A minimum-length tree for the net that uses the channels and takes into account the channel capacities.

(c) The minimum-length tree does not necessarily correspond to minimum delay. If we wish to minimize the delay from terminal A1 to D1, a different tree might be better.



Gate-array global routing.

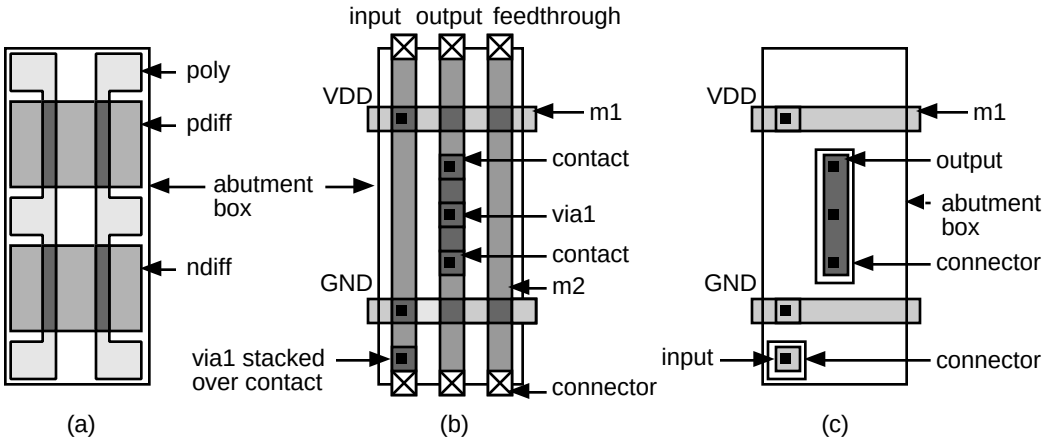
(a) A small gate array.

(b) An enlarged view of the routing. The top channel uses three rows of gate-array base cells; the other channels use only one.

(c) A further enlarged view showing how the routing in the channels connects to the logic cells.

(d) One of the logic cells, an inverter.

(e) There are seven horizontal wiring tracks available in one row of gate-array base cells—the channel capacity is thus 7.

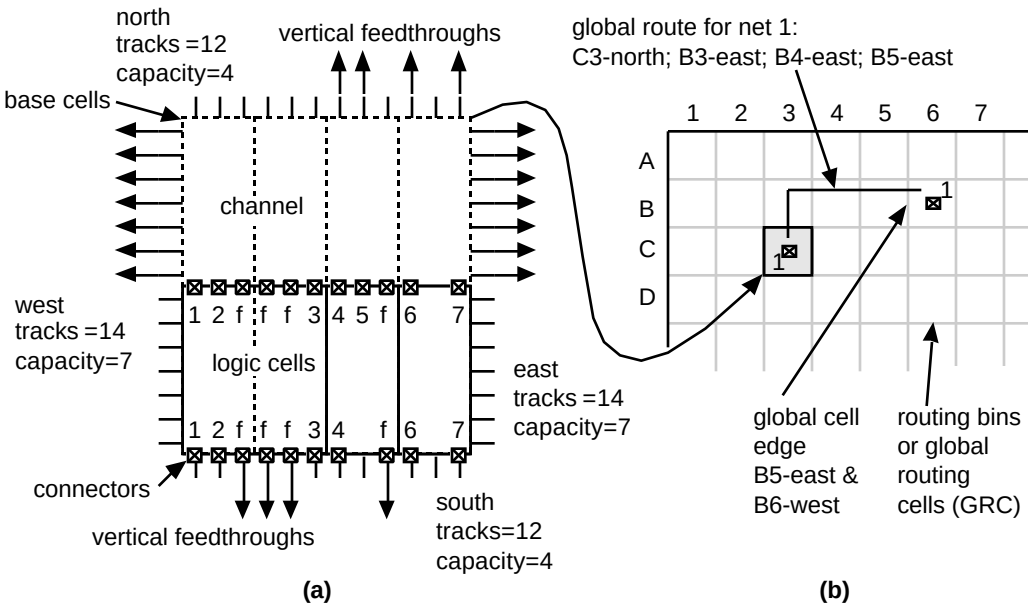


A gate-array inverter

(a) An oxide-isolated gate-array base cell, showing the diffusion and polysilicon layers.

(b) The metal and contact layers for the inverter in a 2LM (two-level metal) process.

(c) The router's view of the cell in a 3LM process.



Global routing a gate array.

(a) A single global-routing cell (GRC or routing bin) containing 2-by-4 gate-array base cells.

For this choice of routing bin the maximum horizontal track capacity is 14, the maximum vertical track capacity is 12.

The routing bin labeled C3 contains three logic cells, two of which have feedthroughs marked 'f'.

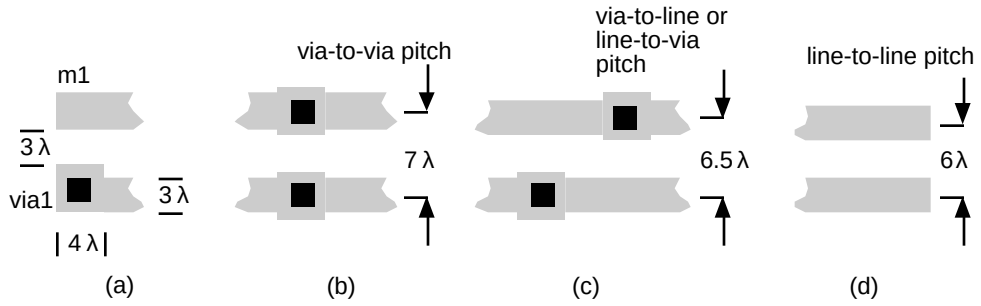
This results in the edge capacities shown.

(b) A view of the top left-hand corner of the gate array showing 28 routing bins.

The global router uses the edge capacities to find a sequence of routing bins to connect the nets.

17.2 Detailed Routing

Key terms and concepts: routing pitch (track pitch, track spacing, or just pitch) • via-to-via (VTV) pitch (or spacing) • via-to-line (VTL or line-to-via) pitch • line-to-line (LTL) pitch. • stitch• waffle via • stacked via • Manhattan routing • preferred direction • preferred metal layer • phantom • blockage map • on-grid • off-grid • trunks • branches • doglegs • pseudoterminals • tracks (like railway tracks) • horizontal track spacing • track spacing • column • column spacing (or vertical track spacing)



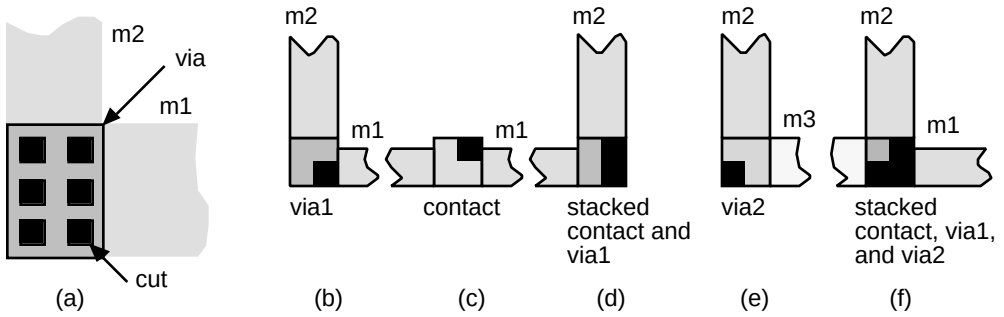
The metal routing pitch.

(a) An example of λ-based metal design rules for m1 and via1 (m1/m2 via).

(b) Via-to-via pitch for adjacent vias.

(c) Via-to-line (or line-to-via) pitch for nonadjacent vias.

(d) Line-to-line pitch with no vias.



Vias

(a) A large m1 to m2 via. The black squares represent the holes (or cuts) that are etched in the insulating material between the m1 and 2 layers.

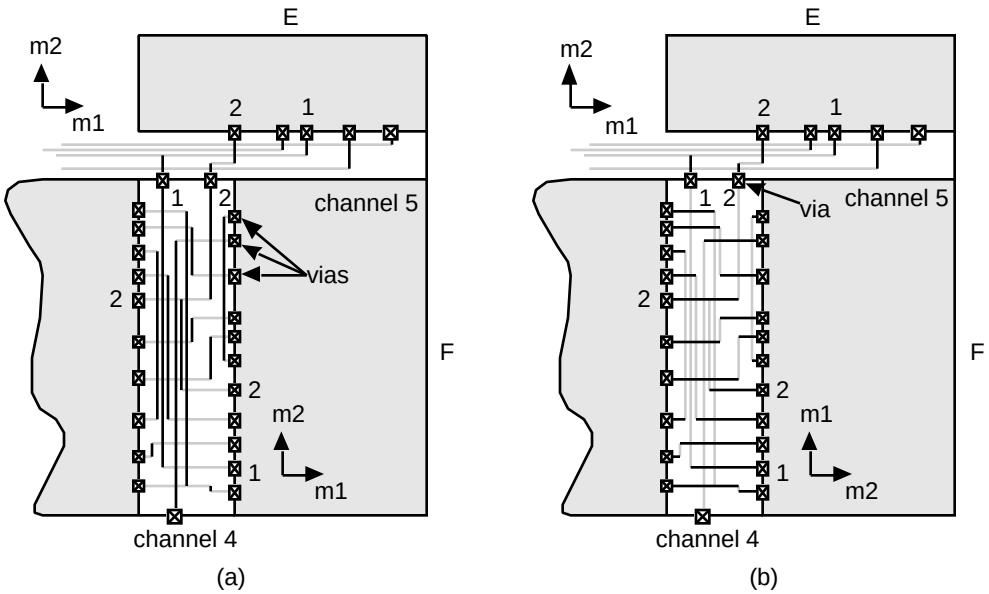
(b) A m1 to m2 via (a via1).

(c) A contact from m1 to diffusion or polysilicon (a contact).

(d) A via1 placed over (or stacked over) a contact.

(e) A m2 to m3 via (a via2).

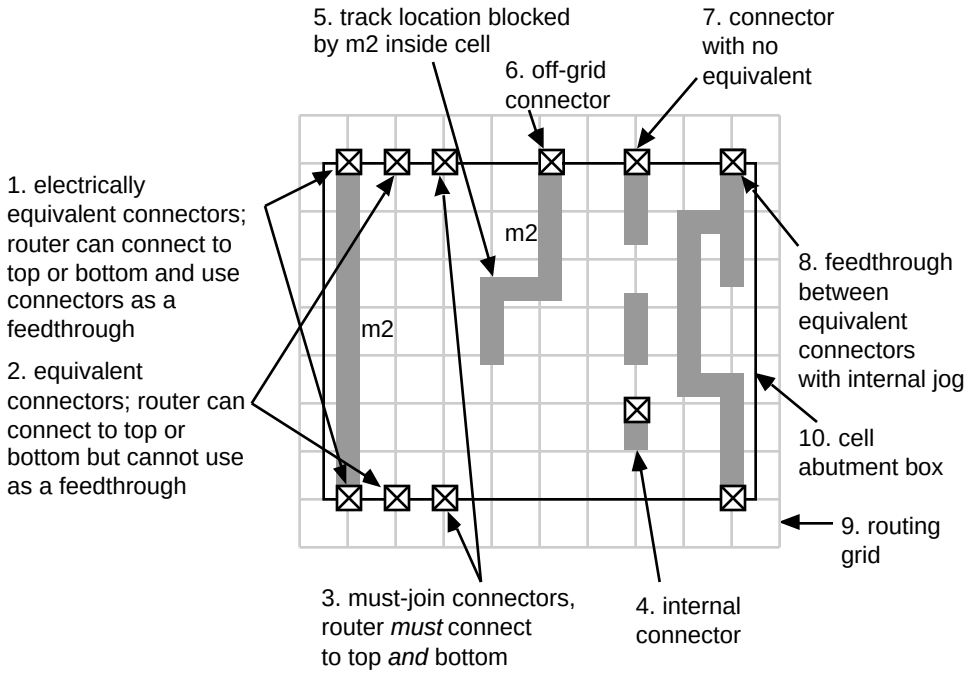
(f) A via2 stacked over a via1 stacked over a contact. Notice that the black square in parts b–c do *not* represent the actual location of the cuts. The black squares are offset so you can recognize stacked vias and contacts.



An expanded view of part of a cell-based ASIC.

(a) Both channel 4 and channel 5 use m1 in the horizontal direction and m2 in the vertical direction. If the logic cell connectors are on m2 this requires vias to be placed at every logic cell connector in channel 4.

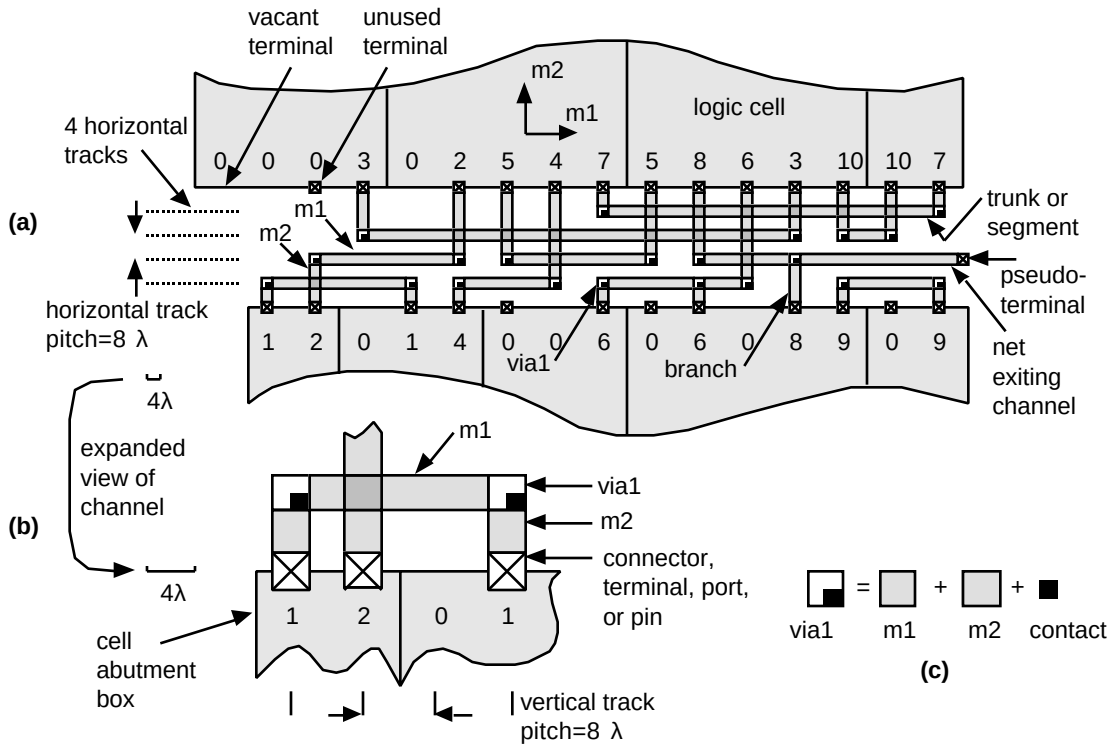
(b) Channel 4 and 5 are routed with m1 along the direction of the channel spine (the long direction of the channel). Now vias are required only for nets 1 and 2, at the intersection of the channels.



The different types of connections that can be made to a cell.

This cell has connectors at the top and bottom of the cell (normal for cells intended for use with a two-level metal process) and internal connectors (normal for logic cells intended for use with a three-level metal process).

The interconnect and connections are drawn to scale.



Terms used in channel routing.

(a) A channel with four horizontal tracks.

(b) An expanded view of the left-hand portion of the channel showing (approximately to scale) how the m1 and m2 layers connect to the logic cells on either side of the channel.

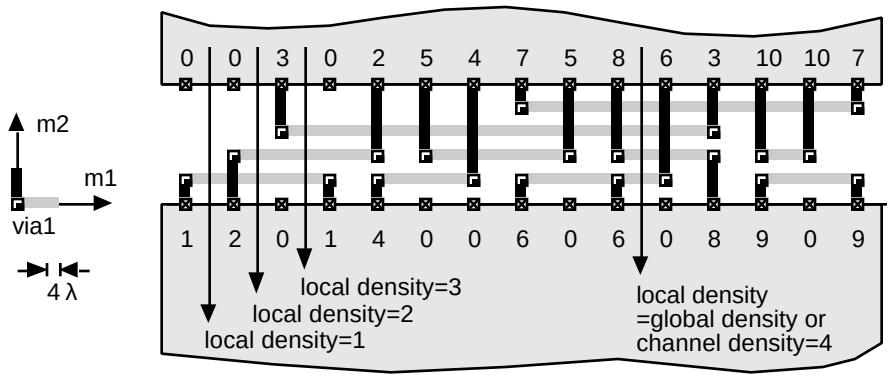
(c) The construction of a via1 (m1/m2 via).

17.2.1 Goals and Objectives

Key terms and concepts: Goal: to complete all the connections between logic cells • Objectives: The total interconnect length and area • The number of layer changes that the connections have to make • The delay of critical paths

17.2.2 Measurement of Channel Density

Key terms and concepts: **local density • global density • channel density**



The definitions of local channel density and global channel density.

Lines represent the m1 and m2 interconnect in the channel to simplify the drawing.

17.2.3 Algorithms

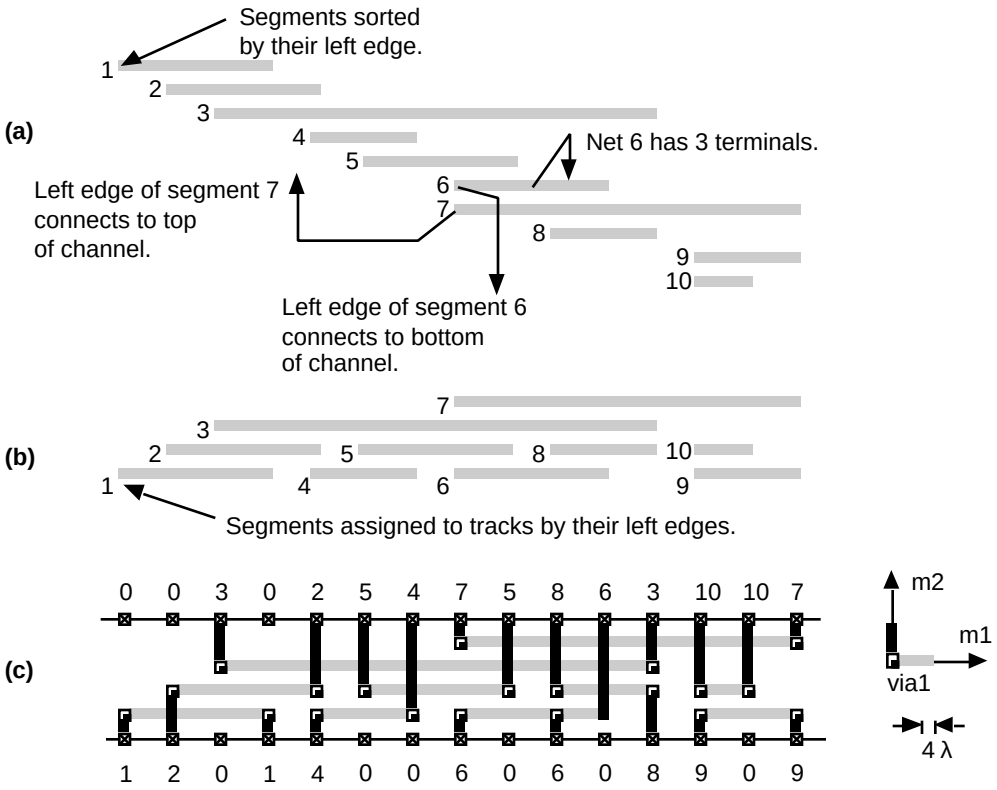
Key terms and concepts: restricted channel-routing problem

17.2.4 Left-Edge Algorithm

Key terms and concepts: left-edge algorithm (LEA)

17.2.5 Constraints and Routing Graphs

Key terms and concepts: vertical constraint • vertical-constraint graph • directed graph • horizontal constraint • horizontal-constraint graph • vertical-constraint cycle (or cyclic constraint) • dogleg router • overlap • overlap capacitance • coupling capacitance • overlap capacitance • channel-routing compaction

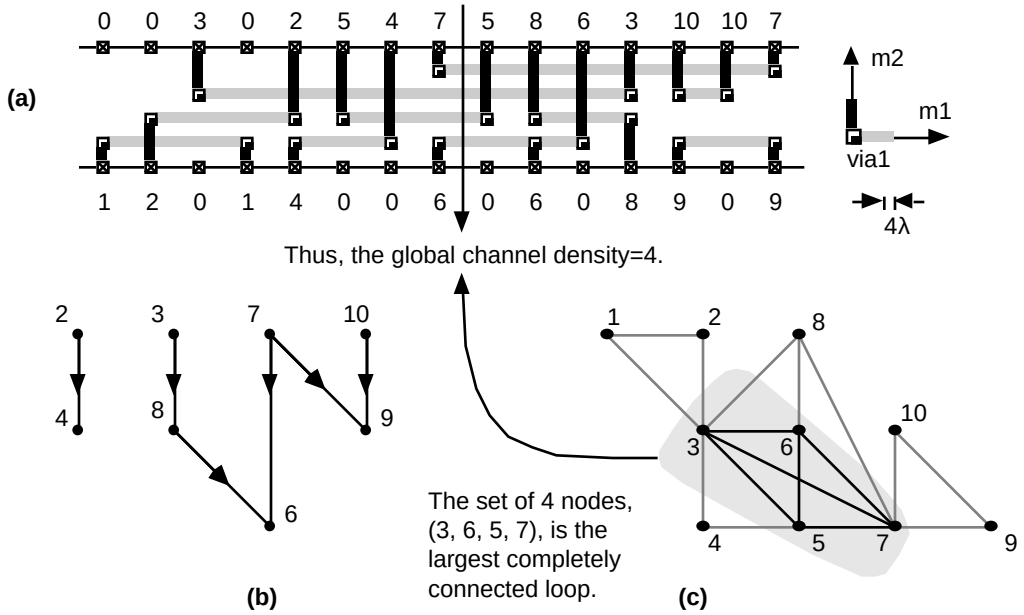


Left-edge algorithm.

(a) Sorted list of segments.

(b) Assignment to tracks.

(c) Completed channel route (with m1 and m2 interconnect represented by lines).



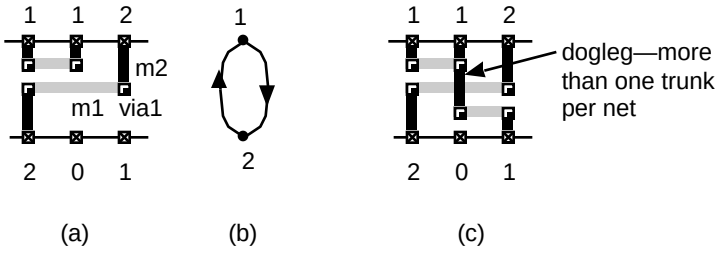
Routing graphs.

(a) Channel with a global density of 4.

(b) The vertical constraint graph. If two nets occupy the same column, the net at the top of the channel imposes a vertical constraint on the net at the bottom. For example, net 2 imposes a vertical constraint on net 4. Thus the interconnect for net 4 must use a track above net 2.

(c) Horizontal-constraint graph. If the segments of two nets overlap, they are connected in the horizontal-constraint graph. This graph determines the global channel density.

The addition of a dogleg, an extra trunk, in the wiring of a net can resolve cyclic vertical constraints.



17.2.6 Area-Routing Algorithms

Key terms and concepts: grid-expansion • maze-running • line-search • **Lee maze-running algorithm• wave propagation • Hightower algorithm • line-search algorithm** (or **line-probe algorithm**) • **escape line • escape point**

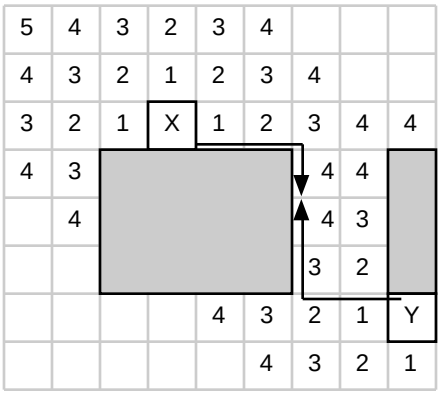
The Lee maze-running algorithm.

The algorithm finds a path from source (X) to target (Y) by emitting a wave from both the source and the target at the same time.

Successive outward moves are marked in each bin.

Once the target is reached, the path is found by backtracking (if there is a choice of bins with equal labeled values, we choose the bin that avoids changing direction).

(The original form of the Lee algorithm uses a single wave.)

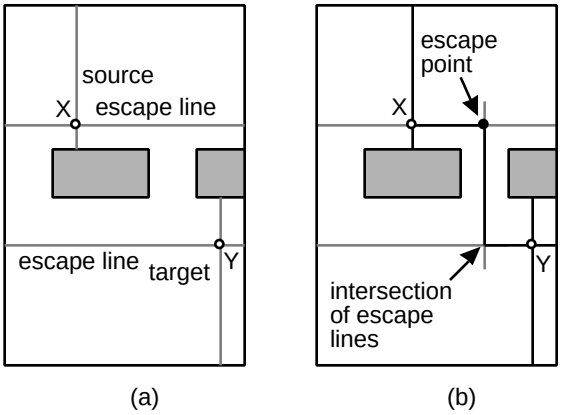


Hightower area-routing algorithm.

(a) Escape lines are constructed from source (X) and target (Y) toward each other until they hit obstacles.

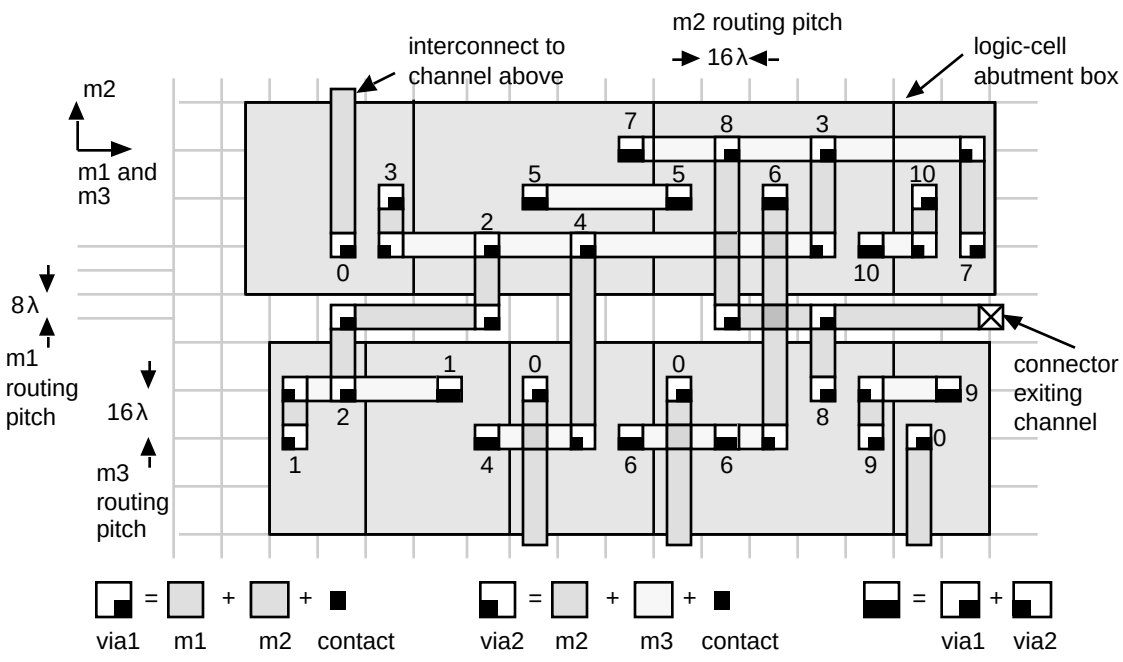
(b) An escape point is found on the escape line so that the next escape line perpendicular to the original misses the next obstacle.

The path is complete when escape lines from source and target meet.



17.2.7 Multilevel Routing

Key terms and concepts: **two-layer routing • 2.5-layer routing • three-layer routing • reserved-layer routing • unreserved-layer routing • HVH routing • VHV routing • multilevel routing • cell porosity**



Three-level channel routing.

In this diagram the m2 and m3 routing pitch is set to twice the m1 routing pitch.

Routing density can be increased further if all the routing pitches can be made equal—a difficult process challenge.

17.2.8 Timing-Driven Detailed Routing

Key terms and concepts: the global router has already set the path the interconnect will follow and little can be done to improve timing • reduce the number of vias • alter the interconnect width to optimize delay • minimize overlap capacitance • gains are small • high-frequency clock nets are **chamfered** (rounded) to match impedances at branches and control reflections at corners.

17.2.9 Final Routing Steps

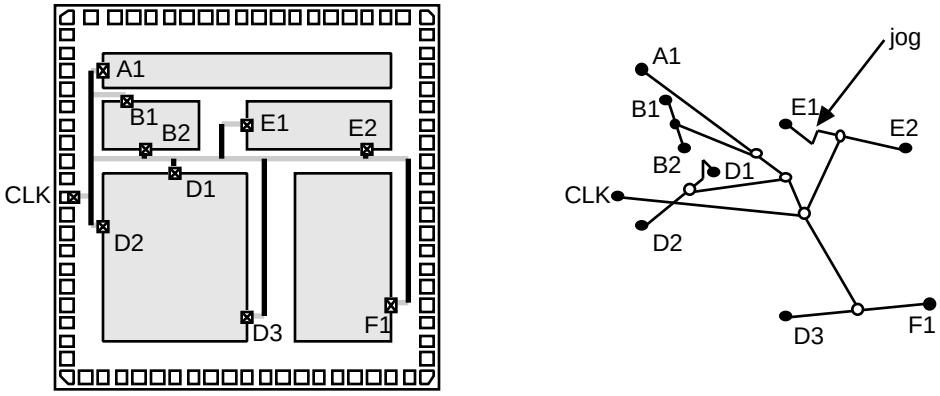
Key terms and concepts: unroutes • rip-up and reroute• engineering change orders (ECO)• via removal• routing compaction

17.3 Special Routing

Key terms and concepts: clock and power nets

17.3.1 Clock Routing

Key terms and concepts: **clock-tree synthesis • clock-buffer insertion • activity-induced clock skew**



Clock routing.

(a) A clock network for a cell-based ASIC.

(b) Equalizing the interconnect segments between CLK and all destinations (by including jogs if necessary) minimizes clock skew.

17.3.2 Power Routing

Key terms and concepts: power-bus sizing • metal electromigration • power simulation • mean time to failure (MTTF) • metallization reliability rules • maximum metal-width rules (fat-metal rules) • die attach • power grid • end-cap cells • routing bias • flip and abut

Metallization reliability rules for a typical 0.5 micron (λ=0.25μm) CMOS process.

Layer/contact/via	Current limit	Metal thickness	Resistance
m1	1mA μm^{-1}	7000Å	95mΩ/square
m2	1mA μm^{-1}	7000Å	95mΩ/square
m3	2 mA μm^{-1}	12,000Å	48mΩ/square
0.8µm square m1 contact to diffusion	0.7 mA		11Ω
0.8µm square m1 contact to poly	0.7mA		16Ω
0.8µm square m1/m2 via (via1)	0.7mA		3.6Ω
0.8µm square m2/m3 via (via2)	0.7mA		3.6Ω

17.4 Circuit Extraction and DRC

Key terms and concepts: circuit-extraction • design-rule check • Dracula deck • design rule violations

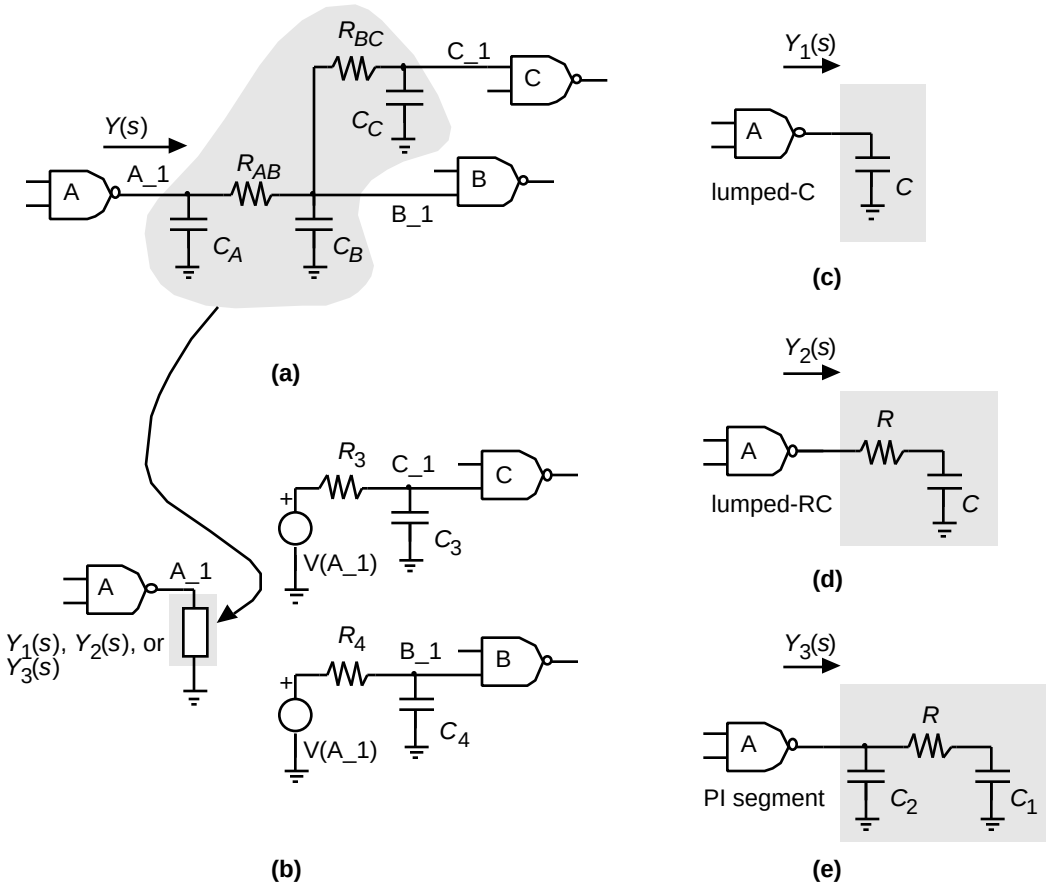
17.4.1 SPF, RSPF, and DSPF

Key terms and concepts: standard parasitic format (SPF) • regular SPF • reduced SPF • detailed SPF

Parasitic capacitances for a typical 1 μm (λ = 0.5 μm) three-level metal CMOS process.

Element	Area/fF μm^{-2}	Fringing/fF μm^{-1}
poly (over gate oxide) to substrate	1.73	NA
poly (over field oxide) to substrate	0.058	0.043
m1 to diffusion or poly	0.055	0.049
m1 to substrate	0.031	0.044
m2 to diffusion	0.019	0.038
m2 to substrate	0.015	0.035
m2 to poly	0.022	0.040
m2 to m1	0.035	0.046
m3 to diffusion	0.011	0.034
m3 to substrate	0.010	0.033
m3 to poly	0.012	0.034
m3 to m1	0.016	0.039
m3 to m2	0.035	0.049
n+ junction (at 0V bias)	0.36	NA
p+ junction (at 0V bias)	0.46	NA

```
#Design Name : EXAMPLE1
#Date : 6 August 1995
#Time : 12:00:00
#Resistance Units : 1 ohms
#Capacitance Units : 1 pico farads
#Syntax :
#N <netName>
#C <capVal>
# F <from CompName> <fromPinName>
# GC <conductance>
# |
# REQ <res>
# GRC <conductance>
# T <toCompName> <toPinName> RC <rcConstant> A <value>
# |
```



The regular and reduced standard parasitic format (SPF) models for interconnect.

(a) An example of an interconnect network with fanout. The driving-point admittance of the interconnect network is $Y(s)$.

(b) The SPF model of the interconnect.

(c) The lumped-capacitance interconnect model.

(d) The lumped-RC interconnect model.

(e) The PI segment interconnect model (notice the capacitor nearest the output node is labeled C_2 rather than C_1). The values of C, R, C_1, and C_2 are calculated so that $Y_1(s)$, $Y_2(s)$, and $Y_3(s)$ are the first-, second-, and third-order Taylor-series approximations to $Y(s)$.

```
# RPI <res>
# C1 <cap>
# C2 <cap>
```

```
# GPI <conductance>
# T <toCompName> <toPinName> RC <rcConstant> A <value>
# TIMING.ADMITTANCE.MODEL = PI
# TIMING.CAPACITANCE.MODEL = PP
N CLOCK
C 3.66
  F ROOT Z
  RPI 8.85
  C1 2.49
  C2 1.17
  GPI = 0.0
  T DF1 G RC 22.20
  T DF2 G RC 13.05


* Design Name : EXAMPLE1
* Date : 6 August 1995
* Time : 12:00:00
* Resistance Units : 1 ohms
* Capacitance Units : 1 pico farads
*| RSPF 1.0
*| DELIMITER "_"
.SUBCKT EXAMPLE1 OUT IN
*| GROUND_NET VSS
* TIMING.CAPACITANCE.MODEL = PP
*|NET CLOCK 3.66PF
*|DRIVER ROOT_Z ROOT Z
*|S (ROOT_Z_OUTP1 0.0 0.0)
R2 ROOT_Z ROOT_Z_OUTP1 8.85
C1 ROOT_Z_OUTP1 VSS 2.49PF
C2 ROOT_Z VSS 1.17PF
*|LOAD DF2_G DF1 G
*|S (DF1_G_INP1 0.0 0.0)
E1 DF1_G_INP1 VSS ROOT_Z VSS 1.0
R3 DF1_G_INP1 DF1_G 22.20
C3 DF1_G VSS 1.0PF
*|LOAD DF2_G DF2 G
*|S (DF2_G_INP1 0.0 0.0)
E2 DF2_G_INP1 VSS ROOT_Z VSS 1.0
R4 DF2_G_INP1 DF2_G 13.05
C4 DF2_G VSS 1.0PF
*Instance Section
XDF1 DF1_Q DF1_QN DF1_D DF1_G DF1_CD DF1_VDD DF1_VSS DFF3
XDF2 DF2_Q DF2_QN DF2_D DF2_G DF2_CD DF2_VDD DF2_VSS DFF3
XROOT ROOT_Z ROOT_A ROOT_VDD ROOT_VSS BUF
```

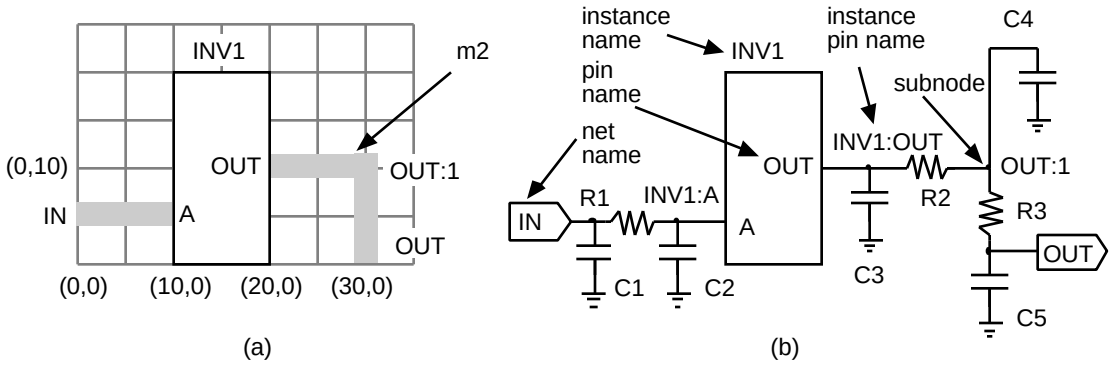
```
.ENDS
.END


.SUBCKT BUFFER OUT IN
* Net Section
*|GROUND_NET VSS
*|NET IN 3.8E-01PF
*|P (IN I 0.0 0.0 5.0)
*|I (INV1:A INV A I 0.0 10.0 5.0)
C1 IN VSS 1.1E-01PF
C2 INV1:A VSS 2.7E-01PF
R1 IN INV1:A 1.7E00
*|NET OUT 1.54E-01PF
*|S (OUT:1 30.0 10.0)
*|P (OUT O 0.0 30.0 0.0)
*|I (INV:OUT INV1 OUT O 0.0 20.0 10.0)
C3 INV1:OUT VSS 1.4E-01PF
C4 OUT:1 VSS 6.3E-03PF
C5 OUT VSS 7.7E-03PF
R2 INV1:OUT OUT:1 3.11E00
R3 OUT:1 OUT 3.03E00
*Instance Section
XINV1 INV:A INV1:OUT INV
.ENDS
```

17.4.2 Design Checks

Key terms and concepts: design-rule check (DRC)• phantom-level DRC• hard layout• Dracula deck • layout versus schematic (LVS)

17.4.3 Mask Preparation

Key terms and concepts: maskwork symbol (M inside a circle) • copyright symbol (C inside a circle)• kerf • scribe lines • edge-seal structures• Caltech Intermediate Format (CIF, a public domain text format) • GDSII Stream (Calma Stream, Cadence Stream)• fab• mask shop• grace value• sizing or mask tooling• tooling specification• mask bias• bird’s beak effect• glass masks or reticles • spot size • critical layers • optical proximity correction (OPC)



The detailed standard parasitic format (DSPF) for interconnect representation.

(a) An example network with two m2 paths connected to a logic cell, INV1. The grid shows the coordinates.

(b) The equivalent DSPF circuit corresponding to the DSPF file in the text.

17.5 Summary

Key terms and concepts:

- Routing is divided into global and detailed routing.
- Routing algorithms should match the placement algorithms.
- Routing is not complete if there are unroutes.
- Clock and power nets are handled as special cases.
- Clock-net widths and power-bus widths must usually be set by hand.
- DRC and LVS checks are needed before a design is complete.