

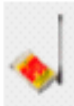
Go Reconfigure

By Dragos Popescu

FPGA's Are Everywhere

- Wireless Networks

- Base stations
 - Pre-distortion
 - Baseband functionality
- 802.16 - UWB



- Wired Networks

- Serial backplanes
- Line card solutions
 - Metro/Edge Routers
 - Edge Access
 - CMTS, DSLAMs
 - IP Routers



- Storage

- Fabric Attached Storage
 - NAS and SANs



- Consumer

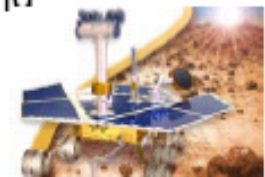
- Digital Displays
- Handsets
- Home Networking



- Automotive Telematics

- Industrial

- Medical Imaging - Ultrasound
- Industrial Automation



- Military and Surveillance

- Transformational Communications

- Next Generation Broadband

- FTTH, VDSL, SHDSL

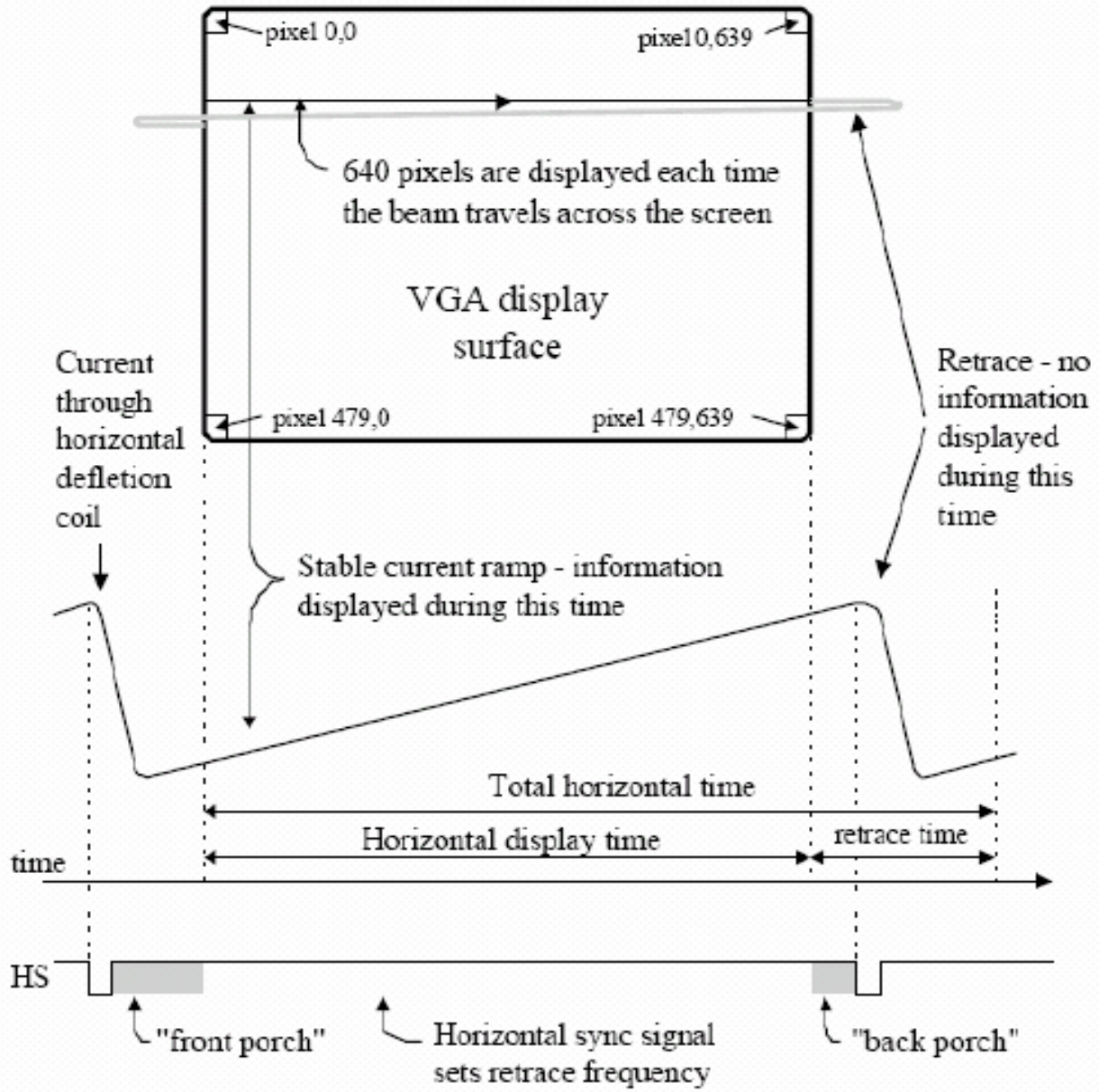
- Video Broadcast (Studio)



Same device - more functions

- VGA Controller
 - PS/2 Controller
 - Chess game
 - Windowing Operators
- Incoming:
- 10Base-T Controller
 - USB Interface
 - Webcam Controller

Rank Order Filter
Morphological Operators
Convolution



```
module VGATestTop(clk, hsync, vsync, r1, r0, g1, g0, b1, b0);
    input clk;

    output hsync;
    output vsync;
    output r1, r0, g1, g0, b1, b0;
    wire r1, r0, g1, g0, b1, b0;

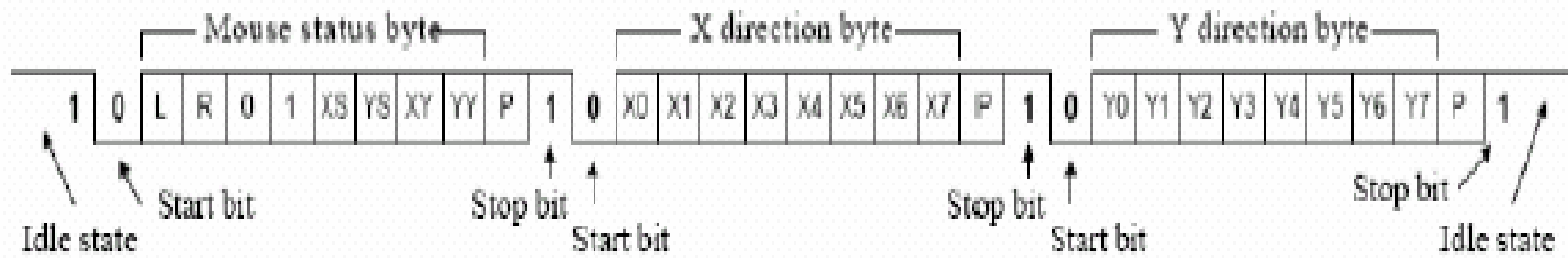
    wire active;
    wire [11:0] x;
    wire [11:0] y;

    VGATimer #(800,64,120,56, 600,23,6,37, 1) timer (clk, hsync, vsync, active, x, y);

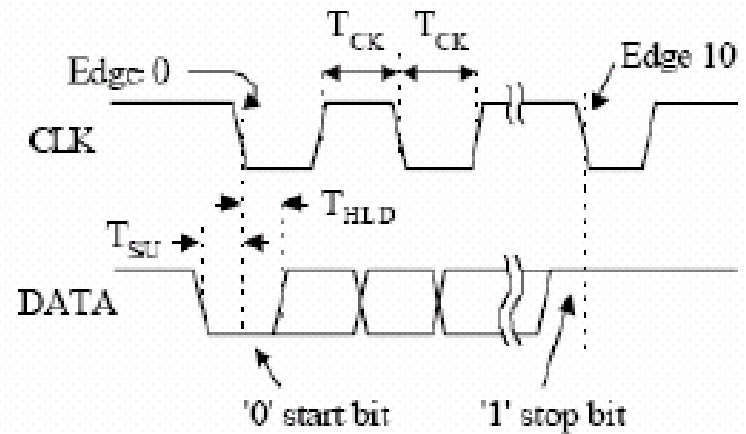
    assign r1 = active&&( ~(x[0]^y[0]));
    assign r0 = active&&( ~(x[1]^y[1]));
    assign g1 = active&&( ~(x[2]^y[2]));
    assign g0 = active&&( ~(x[3]^y[3]));
    assign b1 = active&&( ~(x[4]^y[4]));
    assign b0 = active&&( ~(x[5]^y[5]));

endmodule
```

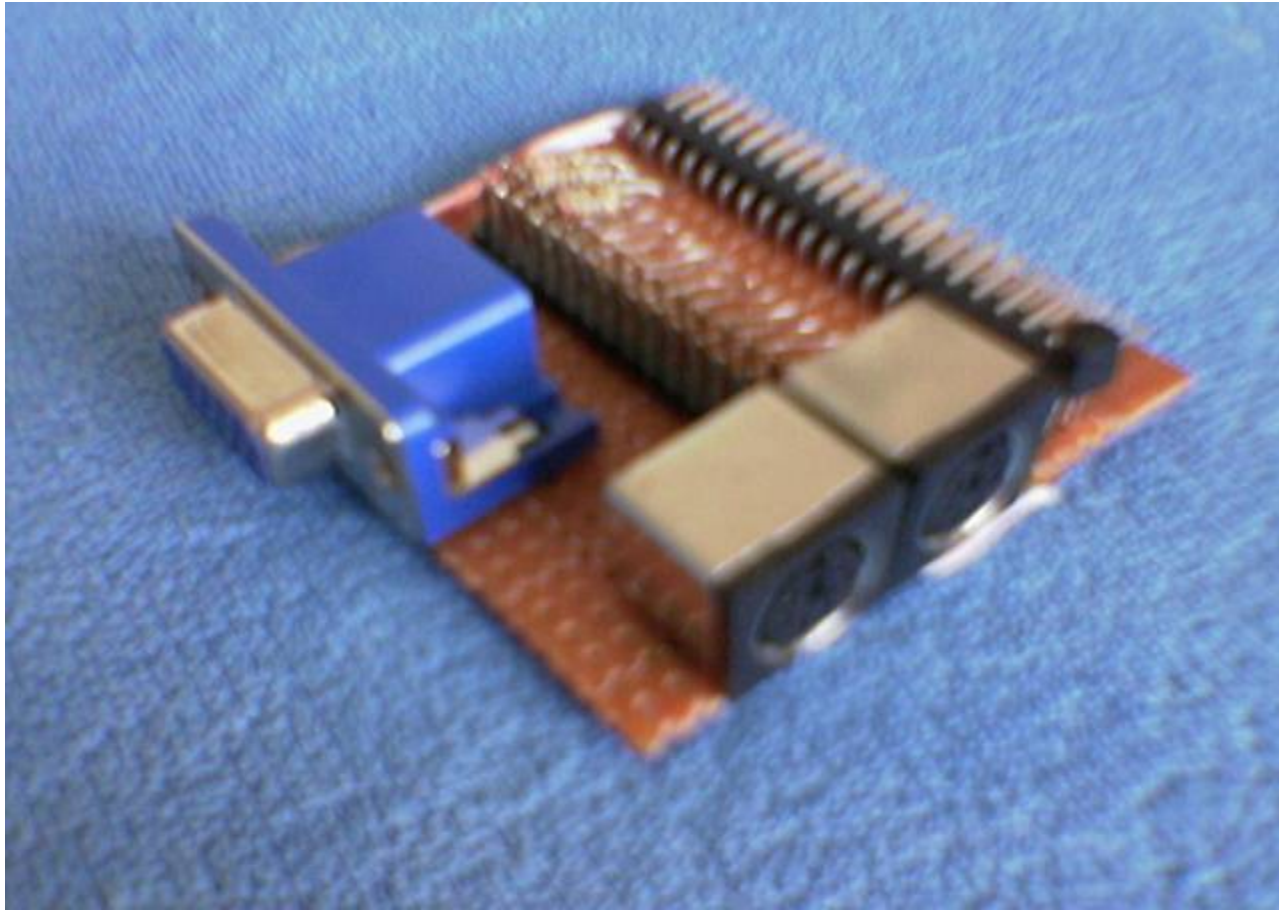


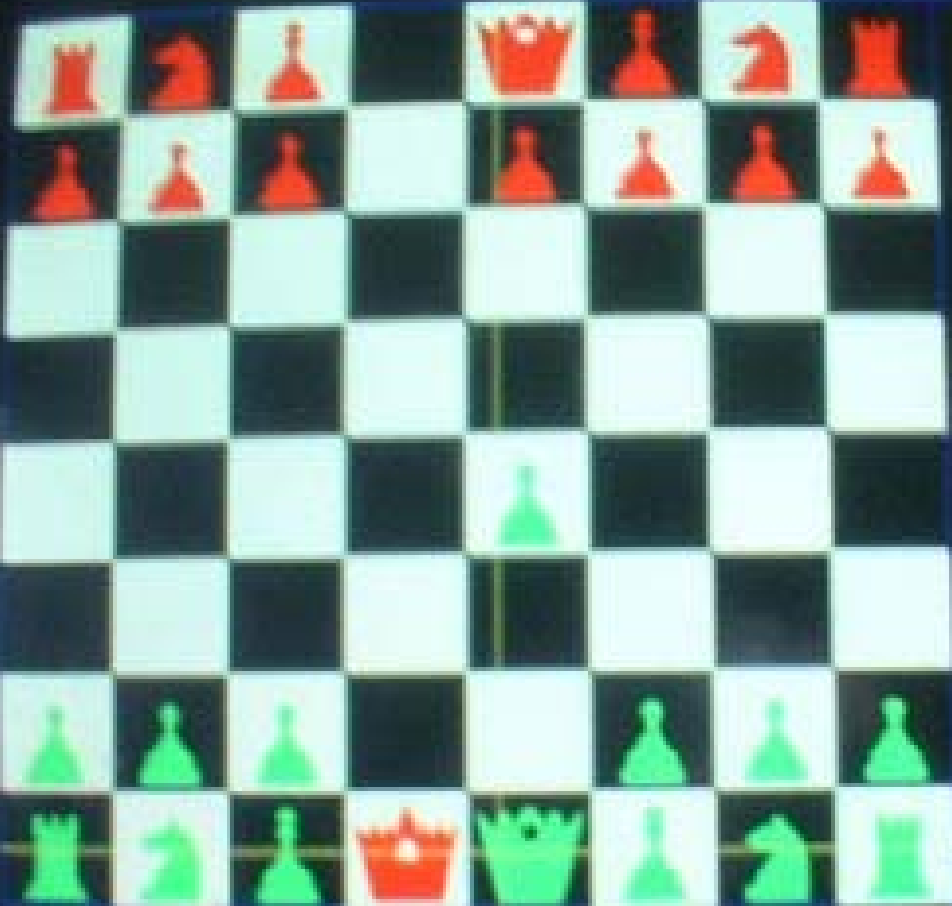


Symbol	Parameter	Min	Max
T_{CK}	Clock time	30us	50us
T_{SU}	Data-to-clock setup time	5us	25us
T_{HLD}	Clock-to-data hold time	5us	25us



VGA & PS/2 Ports

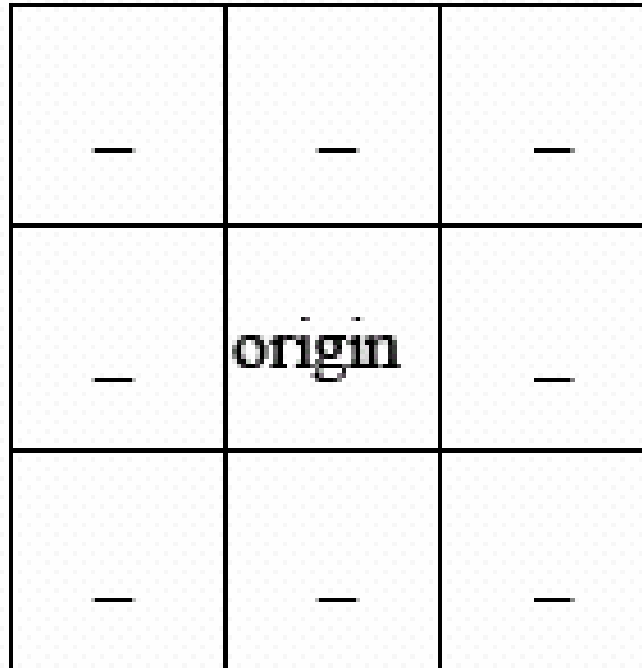




00:01:09 00:00:15

FPGA Chess Demo
by Dragos Popescu

Introduction to Windowing Operators



Pixel Window and Origin

The Algorithms

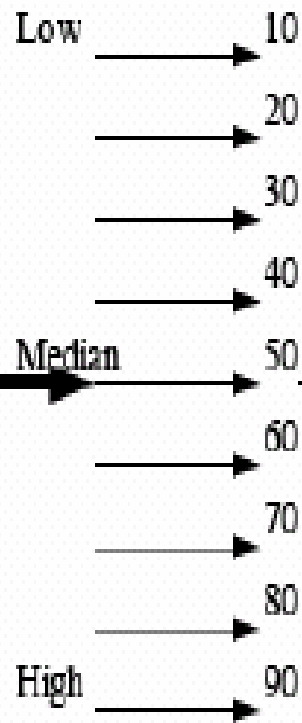
- **Rank Order Filter**
- **Morphological Operators**
- **Convolution**

Rank Order Filter

Input Window:

50	10	20
30	70	90
40	60	80

Sorter Output:



For a RO filter with
Order = 5 (median)

Output Pixel:

-	-	-
-	50	-
-	-	-

Input Image



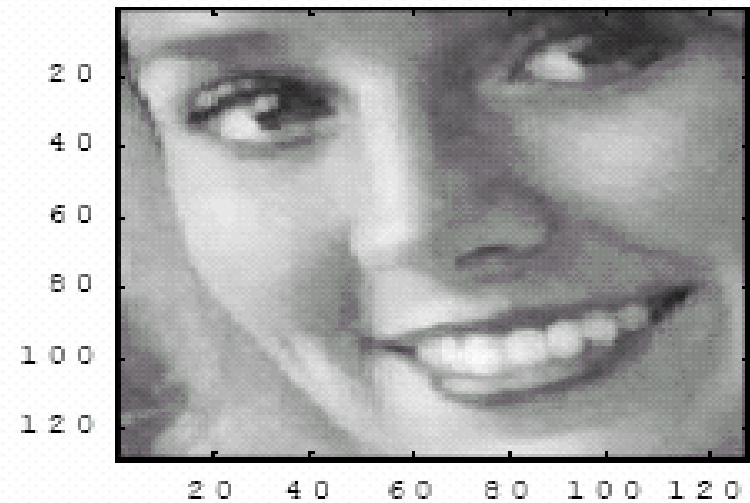
Filtered Image, Order = 2



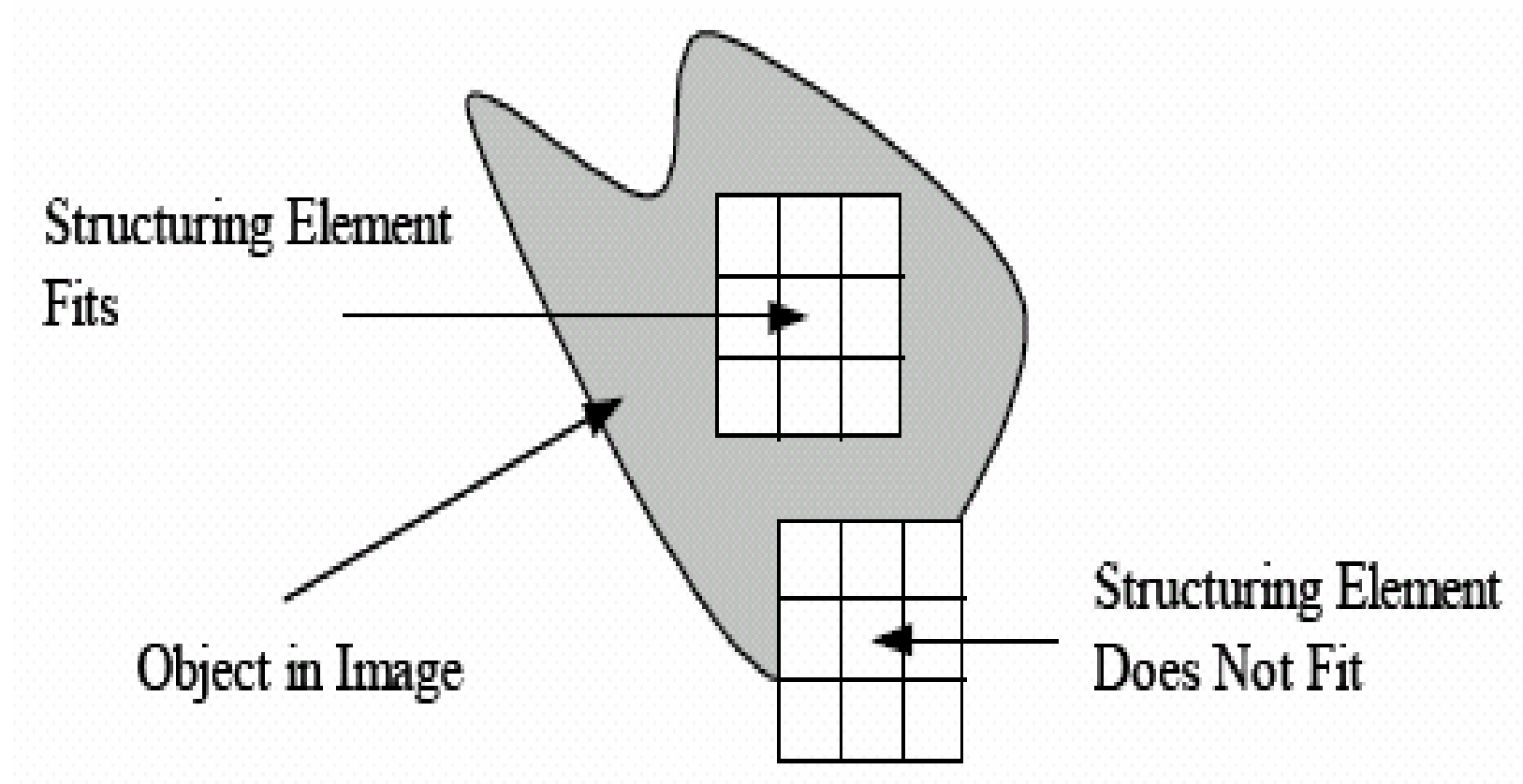
Filtered Image, Order = 5



Filtered Image, Order = 8



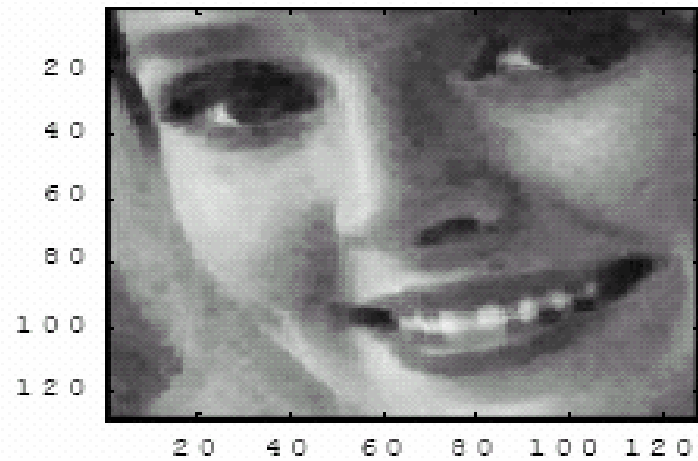
Morphological Operators



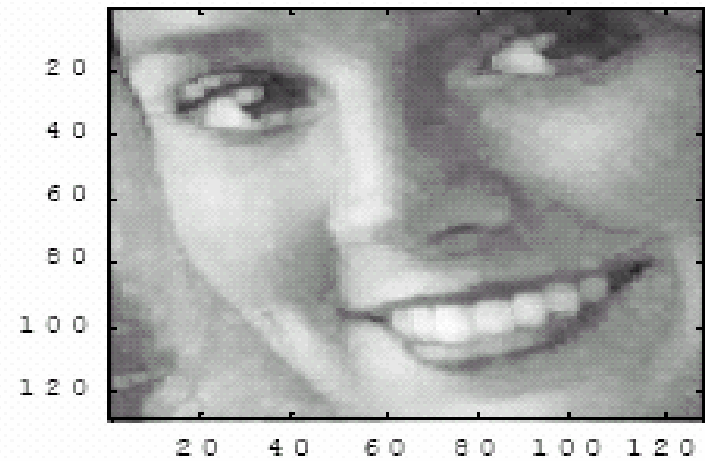
Input Image



Erosion of Input Image



Dilation of Input Image



Convolution

Input Window:

50	10	20
30	70	90
40	60	80

Convolution Mask:

1	1	1
1	2	1
1	1	1



Output Pixel:

-	-	-
-	58	-
-	-	-

Convolution Output = $(50*1 + 10*1 + 20*1 + 30*1 + 70*2 + 90*1 + 40*1 + 60*1 + 80*1)/9 = 57.7778 \Rightarrow 58$

IP/UDP over Ethernet

```
C:\>ipconfig /all

Windows IP Configuration

    Host Name . . . . . : Duron
    Primary Dns Suffix . . . . . :
    Mode Type . . . . . : Unknown
    IP Routing Enabled. . . . . : No
    WINS Proxy Enabled. . . . . : No

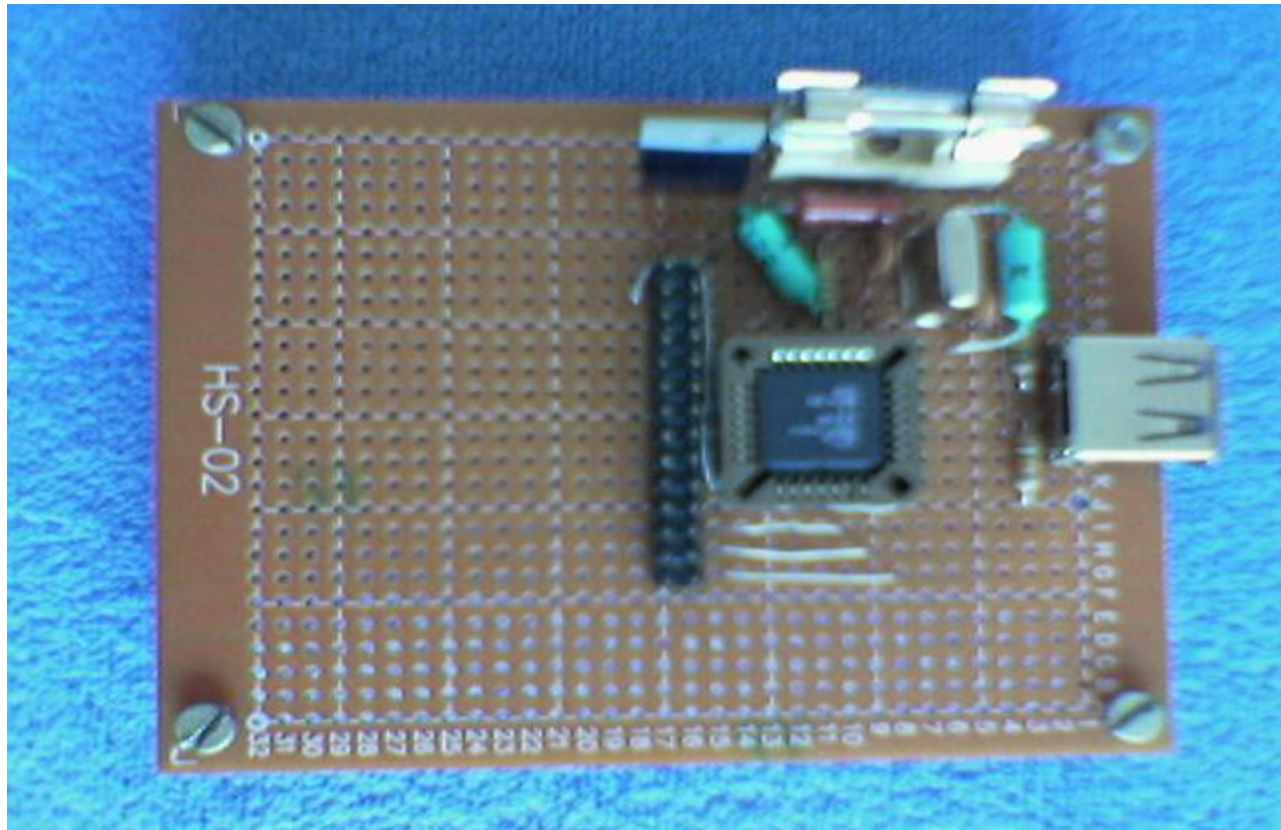
Ethernet adapter Local Area Connection:

    Connection-specific DNS Suffix . :
    Description . . . . . : PCI Fast Ethernet Adapter

    Physical Address. . . . . : 00-07-95-0B-FB-AF ←
    Dhcp Enabled. . . . . : Yes
    Autoconfiguration Enabled . . . . : Yes
    IP Address. . . . . : 192.168.0.2 ←
    Subnet Mask . . . . . : 255.255.255.0
```

```
Waiting for packets (Press Ctrl-C to exit)...
Received 18 bytes from 192.168.0.44
00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11
Received 18 bytes from 192.168.0.44
00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11
Received 18 bytes from 192.168.0.44
00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11
Received 18 bytes from 192.168.0.44
00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11
```

USB Interface



Webcam Controller



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