13. ASIC Design Concepts: Gate Arrays

Cost Issues

- Design Costs
- Non-recurring Engineering Costs (NRE)
- Manufacturing Costs
Cost Issues: Design Costs

Design Costs reduced by
• raising level of abstraction
• re-use
• powerful synthesis methods

Cost-affecting Decisions:
• System Level:
  – System architecture
  – Communication architecture
• Block-Level:
  – appropriate modeling of control-dominated and data path oriented components

Synthesis:
• High-level Synthesis (allocation, scheduling, binding)
• Logic Synthesis (RTL to logic translation, FSM synthesis, logic optimisation, retiming)
• Layout Synthesis (module generators, PLA generators, Place & Route)

Cost Issues: Manufacturing Costs

...depending on Design Style:

- ASIC
  - Semi Custom
  - Full Custom
    - Cell-based
    - Array-based
      - (synthesized) Standard Cells
      - Macro Cells
      - Gate Arrays
      - FPGAs/PLDs
Gate Arrays – Introduction (1)

Gate Arrays (Masterslices):

• Prefabricated active elements (master)
• Construction of logic functions by personalization (wiring macros from a cell library, intra-cell routing)
• Connection of functional blocks by inter-cell routing in 1...3 layers plus contact/via layers
• Arrangement of gate arrays:
  – row structure
  – island structure
  – matrix of structures (= sea of gates)
• Mixed analog/digital gate arrays

Gate Arrays – Introduction (2)

Gate array floor plan with row structure
Gate Arrays – Introduction (3)

Floor plan for a sea of gates array

IMI Grid Structure (1)

IMI gate array structure
IMI Grid Structure (2)

The figure on the previous slide principally shows the structure of gate arrays of International Microcircuits Inc. (IMI) (single metal layers). The real circuit has 1440 cells. In the figure a reduced number of 40 cells is drawn in order to improve the clarity of the representation.

The gate array consists of the following elements:

- Pad (connection to outside world)
- Buffer devices (drive off-chip load capacitances)
- Distributed power and ground buses
- Underpasses to cross under the power and ground buses without contacting them
- Each point represents a contact (potential interconnection point)

Corner of IMI gate array die
IMI Grid Structure (4)

From the figure on the previous slide the following features can be seen:

• Cells containing transistors are clustered around the $V_{DD}$ and $V_{SS}$ buses

• In each cell four horizontal bars (crossing $V_{DD}$ and $V_{SS}$) can be seen. The thick bar represents a poly underpass while the three thin bars are common poly input lines to an nMOS/pMOS transistor pair

• Between cell columns a column of short horizontal poly underpasses is placed

IMI Grid Structure (5)

Grid representation of IMI gate array
IMI Grid Structure (6)

Explanation of the grid:

a) basic cell
   
   (VSS = GND)
   
   b) internal interconnects
   
   - internal gates = short horizontal poly lines
   
   - internal diffusion = short horizontal diffusion lines
   
   c) basic cell and crossover (poly) block

IMI Grid Structure (7)

Underpass

Metal Power Bars

PolySilicon

Diffusion Areas

3 nMOS Transistors and 3 pMOS Transistors with common Drain/Source Terminal

Routing Channel

with horizontal PolySilicon underpasses (possibility of underpassing (vertical) metal lines in this area)
Explanation of the grid (continued):

d) XR = transistor
   - adjacent nMOS and pMOS transistors have a common drain/source connection
   - contacts for the nMOS source and drain connections are on both sides of the V_{SS} bus (same for pMOS transistors and V_{DD} bus)

e) crossover block interconnects
IMI Grid Structure (10)

Nand Circuit Layout Realisation

CMOS matrix cell

CDI Grid Structure

CDI single metal layer gate array structure
Gate Array Design Flow

Personalization Examples (1)

Personalization of IMI and CDI gate arrays for an inverter:

a) schematic
b) IMI layout
c) IMI layout
d) CDI layout
Personalization Examples (2)

NOR gate on IMI

(a) NOR gate diagram
(b) NOR gate circuit
(c) NOR gate layout

Personalization Examples (3)

Layout of transmission gates (TG):

a) single TG
b) pair of TGs with common output
Qualification of Gate Array Design Style

- **Advantages:**
  - Lower number of individual masks needed
  - Higher number of pieces for uncustomized master (cost reduction)
  - Many others for masters, second source fabrication, libraries and design systems

- **Disadvantages:**
  - Area overhead (by unused transistor cells)
  - Overdimensioned routing channels
  - Larger cell size

→ Advantages dominate for smaller production volumes

Costs: Full Custom vs. Gate Array

- Gate Arrays: Reduction of fixed costs (reduced mask costs)
- Increased per piece costs, since utilisation of transistors is not optimal, therefore larger chip area and less yield, implying larger cost