5. CMOS Inverter

Overview

- Logic levels
- Noise Margin
- CMOS Inverter
  - static behaviour
  - dynamic behaviour

Courtesy Quiller Electronics Limited
Inverter as simplest logic gate

Logic Voltage Levels

- **$V_{OL}$**: Nominal voltage corresponding to a low logic state at the output of a logic gate for $v_i = V_{OH}$. Generally $V_{-} \leq V_{OL}$.
- **$V_{OH}$**: Nominal voltage corresponding to a high logic state at the output of a logic gate for $v_i = V_{OL}$. Generally $V_{OH} \leq V_{+}$.
- **$V_{IL}$**: Maximum input voltage that will be recognised as a low input logic level.
- **$V_{IH}$**: Minimum input voltage that will be recognised as a high input logic level.
Noise Margins

**NM_L**: Noise margin associated with a low input level

\[ \text{NM}_L = V_{IL} - V_{OL} \]

**NM_H**: Noise margin associated with a high input level

\[ \text{NM}_H = V_{OH} - V_{IH} \]

Dynamic Response of Logic Gates

- **Rise time** \( t_r \): time required for the transition from \( V_{10\%} \) to \( V_{90\%} \).
- **Fall time** \( t_f \): time required for the transition from \( V_{90\%} \) to \( V_{10\%} \).

\[ V_{10\%} = V_{OL} + 0.1(V_{OH} - V_{OL}) \]
\[ V_{90\%} = V_{OL} + 0.9(V_{OH} - V_{OL}) \]

- **Propagation delay** \( \tau_{P} \): difference in time between the input and output signals reaching \( V_{50\%} \).

\[ V_{50\%} = \frac{V_{OH} + V_{OL}}{2} \]
\[ \tau_{P} = \frac{\tau_{PLH} + \tau_{PHL}}{2} \]
MOS Inverter with Resistive Load

- NMOS switching device $M_S$ designed to force $v_O$ to $V_{OL}$
- Resistor load $R$ to pull the output up toward the power supply $V_{DD}$
- $V_{OH} = V_{DD}$ (driver in cut off $\Rightarrow i_D = 0$)
- $V_{OL}$ determined by $W/L$ ratio of $M_S$

Example

(a) $V_I = V_{OL} < V_{TH}$

(b) $V_I = V_{OH} = 5V$
On - Resistance

\[ R_{on} = \frac{V_{DS}}{i_D} = \frac{1}{K' \frac{W}{L} \left( V_{GS} - V_{TN} - \frac{V_{DS}}{2} \right)} \]

\[ V_{OL} = V_{DD} \frac{R_{on}}{R_{on} + R} = V_{DD} \frac{1}{1 + \frac{R}{R_{on}}} \]

Transistor Alternatives to the Load Resistor

(a) NMOS inverter with gate of the load device connected to its source

(b) NMOS inverter with gate of the load device grounded

(c) Saturated load inverter

(d) Linear load inverter
**CMOS Inverter Technology**

![Diagram of CMOS Inverter](image)

<table>
<thead>
<tr>
<th>CMOS Transistor Parameters</th>
<th>NMOS Device</th>
<th>PMOS Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{TO} )</td>
<td>1 V</td>
<td>-1 V</td>
</tr>
<tr>
<td>( \gamma )</td>
<td>0.50 ( \sqrt{V} )</td>
<td>0.75 ( \sqrt{V} )</td>
</tr>
<tr>
<td>( 2 \phi_F )</td>
<td>0.60 V</td>
<td>0.70 V</td>
</tr>
<tr>
<td>( K' )</td>
<td>25 ( \mu A/V^2 )</td>
<td>10 ( \mu A/V^2 )</td>
</tr>
</tbody>
</table>

**Complementary MOS (CMOS) Logic Design**

- Inverter with resistive load \( \Rightarrow \) power dissipation when the input is high.
- If an NMOS and PMOS transistor is used \( \Rightarrow \) CMOS.
- One transistor is always off while the other is on \( \Rightarrow \) no static power consumption.
CMOS voltage transfer Characteristic

Regions of Operation of Transistors in a Symmetrical Inverter

<table>
<thead>
<tr>
<th>Region</th>
<th>Input Voltage $v_I$</th>
<th>Output Voltage $v_O$</th>
<th>NMOS Transistor</th>
<th>PMOS Transistor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$v_I \leq V_{TN}$</td>
<td>$V_{OH} = V_{DD}$</td>
<td>Cutoff</td>
<td>Linear</td>
</tr>
<tr>
<td>2</td>
<td>$V_{TN} &lt; v_I \leq v_O + V_{TP}$</td>
<td>High</td>
<td>Saturation</td>
<td>Linear</td>
</tr>
<tr>
<td>3</td>
<td>$v_I \approx V_{DD}/2$</td>
<td>$V_{DD}/2$</td>
<td>Saturation</td>
<td>Saturation</td>
</tr>
<tr>
<td>4</td>
<td>$v_O + V_{TN} &lt; v_I \leq (V_{DD} + V_{TP})$</td>
<td>Low</td>
<td>Linear</td>
<td>Saturation</td>
</tr>
<tr>
<td>5</td>
<td>$v_I \geq (V_{DD} + V_{TP})$</td>
<td>$V_{OL} = 0$</td>
<td>Linear</td>
<td>Cutoff</td>
</tr>
</tbody>
</table>
What happens, if the inverter is not symmetrical?

![Graph showing CMOS inverter with symmetrical and asymmetrical inverters]

Symmetrical inverter \((K_n = K_p)\)

Asymmetrical inverter \((K_R = K_n / K_p)\)

Calculation of \(V_{IL}\)

Equating currents for saturated nMOS and nonsaturated pMOS device (Region 2):

\[
\frac{K_n}{2} (V_{in} - V_{Tn})^2 = \frac{K_p}{2} \left[ 2(V_{DD} - V_{in} - |V_{Tp}|)(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2 \right]
\]

The derivation condition \(dV_{out} / dV_{in} = -1\) has to be evaluated for

\[I_{Dn}(V_{in}) = I_{Dp}(V_{in}, V_{out})\]

\[
\frac{dV_{out}}{dV_{in}} = \left( \frac{dI_{Dn}}{dV_{in}} \right) - \left( \frac{\partial I_{Dp}}{\partial V_{in}} \right) = -1
\]

Evaluating the derivation gives:

\[
V_{IL} \left( 1 + \frac{K_n}{K_p} \right) = 2V_{out} + \frac{K_n}{K_p} V_{Tn} - V_{DD} - |V_{Tp}|
\]

This equation has to be solved together with the first equation \(\Rightarrow V_{IL}\)
Calculation of $V_{IH}$

At the point $V_{IH}$ the NMOS device is nonsaturated and the PMOS transistor is saturated (region 4):

$$\frac{K_n}{2} \left[ 2(V_{IH} - V_{Tn})V_{out} - V_{out}^2 \right] = \frac{K_p}{2} \left( V_{DD} - V_{IH} - |V_{TP}| \right)^2$$

The derivation condition $\left( \frac{dV_{out}}{dV_{in}} \right) = -1$ has to be evaluated for $I_{Dn}(V_{in}, V_{out}) = I_{Dp}(V_{in})$:

$$\frac{dV_{out}}{dV_{in}} = \frac{(dI_{Dp} / dV_{in}) - (\partial I_{Dn} / \partial V_{out})}{\partial I_{Dn} / \partial V_{out}} = -1$$

which gives:

$$V_{IH} \left( 1 + \frac{K_p}{K_n} \right) = 2V_{out} + V_{Tn} + \frac{K_p}{K_n} \left( V_{DD} - |V_{TP}| \right)$$

This equation forms together with the first equation a quadratic in $V_{IH}$ which has to be solved.

Calculation of $V_{th}$

For $V_{th} = V_{in} = V_{out}$ both transistors are saturated ($\lambda$ is assumed to be 0):

$$\frac{K_n}{2} (V_{th} - V_{Tn})^2 = \frac{K_p}{2} \left( V_{DD} - V_{th} - |V_{TP}| \right)^2$$

Solving for $V_{th}$ yields:

$$V_{th} = \frac{V_{Tn} + \sqrt{K_p / K_n (V_{DD} - |V_{TP}|)}}{1 + \sqrt{K_p / K_n}}$$
**Design of CMOS inverter (I)**

- \( NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH} \)
- \( NM_L = V_{IL} - V_{OL} = V_{IL} - 0 = V_{IL} \)
- \( K_R = K_p / K_n \)
- Remember: 
  \[
  K_n = K_n' \left( \frac{W}{L} \right)_n
  \]
  \[
  K_p = K_p' \left( \frac{W}{L} \right)_p
  \]

⇒ Influence of the symmetry via \( W/L \) of transistors!

---

**Design of CMOS inverter (II)**

The ratio \((W/L)\) in CMOS design is used to set the level of \( V_{th} \).

The ratio required to establish a given inverter threshold voltage is:

\[
\begin{align*}
    K_n &= \mu_n (W/L)_n \\
    K_p &= \mu_p (W/L)_p
\end{align*}
\]

To get a symmetrical voltage transfer curve, \( V_{th} \) is set to \( V_{DD}/2 \):

If in a process \(|V_{Tp}| = V_{Tn}|\), the device aspect ratios for a symmetrical inverter are related by:

\[
\begin{align*}
    K_n &= \frac{1}{2} V_{DD} - |V_{Tp}| \\
    K_p &= \frac{1}{2} V_{DD} - V_{Tn}
\end{align*}
\]

\[
\begin{align*}
    (W/L)_n &= \frac{\mu_n}{\mu_p}
\end{align*}
\]

Since \( \mu_n / \mu_p \approx 2.5 \), a minimum area CMOS inverter will have \((W/L)_n \approx 1\) and \((W/L)_p \approx 2.5\). In this case the voltage transfer function is completely symmetric.
Summary

So what did we accomplish until now?

- We know how a CMOS inverter works.
- \( V_{\text{OL}}, V_{\text{OH}} \) - do you still know it?
- We know how to set the W/L ratios of the transistors to get optimal noise margins.
- So we make every inverter the same, that is to say minimal -or?

Dynamic Behavior of the CMOS Inverter
High to Low Output Transition (I)

\( M_N \) goes from Cutoff over Saturation into Nonsaturation region for the given input.
The border between Saturation and Nonsaturation is reached at the time \( t_x \) and the output voltage \( V_{\text{out}} = V_{\text{OH}} - V_{\text{Tn}} \)
High to Low Output Transition (II)

In order to simplify the final expressions, the integrations on the right for computing \( t_{HL} \) are done with the borders from \( V_{DD} \) to \( V_0 \) (\( V_1 = 0.9 \ V_{DD}, \ V_0 = 0.1 \ V_{DD} \))

Saturation:

\[
\begin{align*}
t_x - t_1 &= -\frac{dQ}{dt} \int_{V_{io}}^{V_{io} - V_{Tn}} \frac{dV_{OUT}}{V_{io} - V_{Tn}} = \frac{2C_{out}V_{Tn}}{K_n(V_{DD} - V_{Tn})^2} \\
\int dt &= C_{out} \int \frac{dV_{OUT}}{i}
\end{align*}
\]

Nonsaturation:

\[
\begin{align*}
t_2 - t_x &= -\frac{dQ}{dt} \int_{V_{io}}^{V_{io} - V_{Tn}} \frac{dV_{OUT}}{V_{io} - V_{Tn}} = -\frac{2C_{out}}{K_n} \frac{1}{2(V_{DD} - V_{Tn})} \ln \left( \frac{V_{OUT}}{2(V_{DD} - V_{Tn}) - V_{OUT}} \right)_{V_{io} - V_{Tn}}^V_{V_{io} - V_{Tn}}
\end{align*}
\]

In our case:

\[
\begin{align*}
t_{HL} &= (t_x - t_1) + (t_2 - t_x) \\
\text{therefore: } t_{HL} &= \tau \left[ \frac{2V_{Tn}}{V_{DD} - V_{Tn}} + \ln \left( \frac{2(V_{DD} - V_{Tn})}{V_0} - 1 \right) \right]
\end{align*}
\]

where \( \tau = \frac{C_{out}}{K_n(V_{DD} - V_{Tn})} \)

High to Low Output Transition (III)

We have used the following integral:

\[
\int \frac{dx}{x(a + bx^n)} = \frac{1}{an} \ln \left( \frac{x^n}{a + bx^n} \right)
\]

In our case:

\[
\begin{align*}
n = 1, \ b = -1 \\
\int \frac{dx}{ax - x^2} = \frac{1}{a} \ln \left( \frac{x}{a - x} \right)
\end{align*}
\]

\[
\begin{align*}
t_{HL} &= (t_x - t_1) + (t_2 - t_x) \\
\text{therefore: } t_{HL} &= \tau \left[ \frac{2V_{Tn}}{V_{DD} - V_{Tn}} + \ln \left( \frac{2(V_{DD} - V_{Tn})}{V_0} - 1 \right) \right]
\end{align*}
\]

where \( \tau = \frac{C_{out}}{K_n(V_{DD} - V_{Tn})} \)
Low to high output transition

From symmetry \((V_{Tn} \rightarrow V_{Tp}; K_n \rightarrow K_p)\) follows for the high to low transition time:

\[
\tau_{LH} = \frac{C_{OUT}}{K_p \left(V_{DD} - V_{TP}\right)} \left[ \frac{2V_{TP}}{V_{DD} - V_{TP}} + \ln \left( \frac{2(V_{DD} - V_{TP})}{V_0} - 1 \right) \right]
\]

\[V_{DD} = 5 \text{ V}\]

\[V_0 = 0 \text{ V}\]

\[V_{O(0+)} = 0 \text{ V}\]

Dynamic Behavior of the CMOS Inverter (cont’d)

- The choice of size of the NMOS and PMOS transistors can be dictated by the desired average propagation delay \(\tau_p\)
- For symmetrical inverter:

\[
\tau_p = \frac{t_{PHL} + t_{PLH}}{2} = t_{PHL} = t_{PLH} \quad K'_n \approx 2.5 K'_p
\]

\[t_r = t_f = 2 \tau_p\]

Example:

Symmetrical reference inverter

\[|V_{TP}| = V_{TN} = 1 \text{ V}\]

\[\tau_p = 6.4 \text{ ns}\]

\[C = 1 \text{ pF}\]

\[t_r = t_f = 12.8 \text{ ns}\]

Scaled inverters

a) \(\tau_p = 1 \text{ ns}\)

b) \(\tau_p = 3.2 \text{ ns}\)
Power Dissipation

- Two kinds of power dissipation in digital electronics:
  - static power dissipation (logic gate output is stable)
  - dynamic power dissipation (during switching of logic gate)

- With CMOS nearly no static power dissipation!

Dynamic Power Dissipation (I)

Power dissipation due to charge and discharge of capacitances

The total energy $E_D$ delivered by the source is given by

$$E_D = \int_0^\infty P(t)dt$$

The power $P(t) = V_{DD}i(t)$, and because $V_{DD}$ is a constant,

$$E_D = \int_0^\infty V_{DD}i(t)dt = V_{DD}\int_0^\infty i(t)dt$$

The current supplied by source $V_{DD}$ is also equal to the current in capacitor $C$, and so

$$E_D = V_{DD}\int_0^\infty C\frac{dv_C}{dt}dt$$

$$= CV_{DD}\int_{v_C(0)}^{v_C(\infty)} dv_C$$
Dynamic Power Dissipation (II)

Integrating from $t = 0$ to $t = \infty$, with $V_C(0) = 0$ and $V_C(\infty) = V_{DD}$ results in

$$E_D = CV_{DD}^2$$

We know that the energy $E_s$ stored in capacitor $C$ is given by

$$E_s = \frac{CV_{DD}^2}{2}$$

and thus the energy $E_L$ lost in the resistive element must be

$$E_L = E_D - E_s = \frac{CV_{DD}^2}{2}$$

The total energy $E_{TD}$ dissipated in the process of first charging and then discharging the capacitor is equal to

$$E_{TD} = \left( \frac{CV_{DD}^2}{2} \right)_{\text{Charge}} + \left( \frac{CV_{DD}^2}{2} \right)_{\text{Discharge}}$$

$$= CV_{DD}^2$$

Dynamic Power Dissipation (III)

Thus, every time a logic gate goes through a complete switching cycle, the transistors within the gate dissipate an energy equal to $E_{TD}$. Logic gates normally switch states at some relatively high frequency (switching events/second), and the dynamic power $P_D$ dissipated by the logic gate is then

$$P_D = CV_{DD}^2 f$$

In effect, an average current equal to $(CV_{DD} f)$ is supplied from the source $V_{DD}$. 
Dynamic Power Dissipation (IV)

• Power dissipation due to the “short circuit current” (when both transistors are on during transition)
• The short circuit current reaches a peak for $V_{in} = V_{out} = V_{DD}/2$

Summary

Let’s repeat:

• What is the dynamic behaviour of the inverter?
• What do we need it for?
• What kind of power dissipation is there?
• What kind of power dissipation is dominant with CMOS logic?

$$P_D = CV_{DD}^2 f$$