15 Silicon On Insulator

1. Introduction

The use of Silicon-On-Insulator (SOI) technology, illustrated in figure 15-xxx, is bringing interesting new possibilities compared to conventional bulk technology. A slowing of the rate of progress in CMOS bulk technology has highlighted recently the extra performance offered by SOI. Performance improvements concern the power consumption and the commutation speed. In the best case, the SOI technology may cut the power consumption nearly by half, with speed improvements close to 30%. The speed improvement itself is equivalent to about two years of progress in bulk CMOS technology.

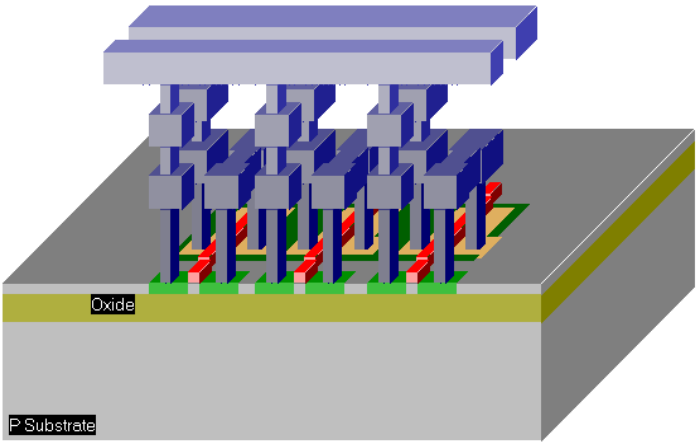


Fig. 15-xxx : 3D View of SOI ring inverter showing the SiO2 buried layer(inv3Soi.MSK)

In fact, the SOI technology has been available for more than 20 years, but its applications were mainly restricted to space and army due to very low sensitivity to radiation. The route to commercial use of SOI still faces several issues: one is the cost of the substrate, which is 5 to 10 times the cost of a bulk wafer, an other is the needs to train designers to specific design techniques and rules, as the behavior of a SOI MOS device differs slightly from the bulk MOS device.

The SOI Substrate

SOI refers to placing a thin layer of silicon on top of a silicon oxide insulator, as illustrated in figure 15-xxx. The transistors are built on top of this thin layer of SOI. A 0.12µm SOI technology, namely "soi012.RUL" is available in Microwind. It enables the comparative simulation with the corresponding bulk technology (cmos012.rul, the standard CMOS 0.12µm technology).

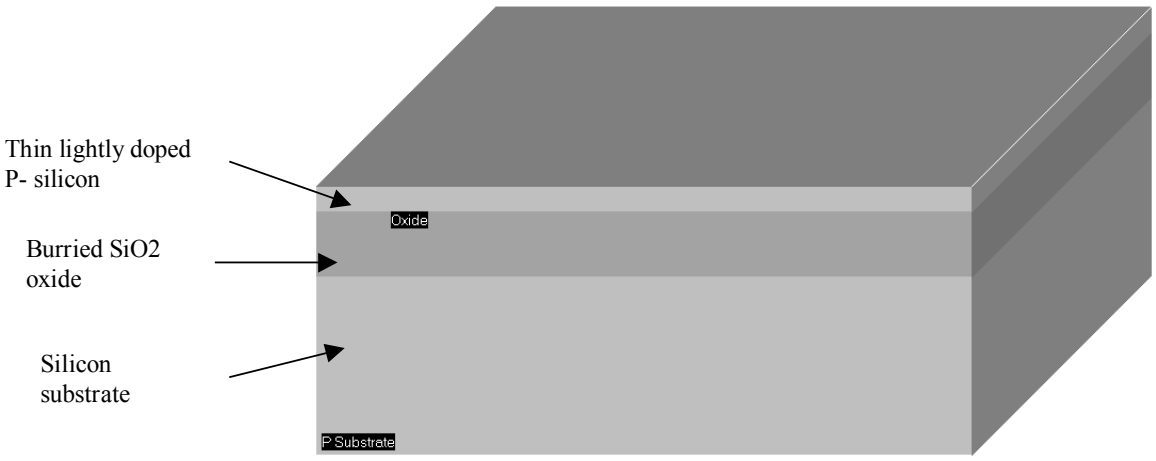


Fig. 15-xxx : 3D View of SOI ring inverter showing the SiO2 buried layer(inv3Soi.MSK)

The basic idea is that the SOI layer will reduce the parasitic junction capacitance of the switch, so it will operate faster. Every time the transistor is turned on, it must first charge all its internal capacitance before it can begin to switch. Among these parasitic capacitances are the junction capacitance Csb and Cdb, which are strongly reduced by the silicon dioxide, as described in the two-dimensional cross-section of figure 15-xxx. The thicker the Sio2 oxide, the smaller the parasitic capacitance. The typical insulator thickness is between 200 and 500nm. In the SOI CMOS 0.12µm technology provided with Microwind, the dielectric thickness is 300nm, and the silicon thickness is 150nm. Consequently, the SOI technology enables the MOS device to operate significantly faster.

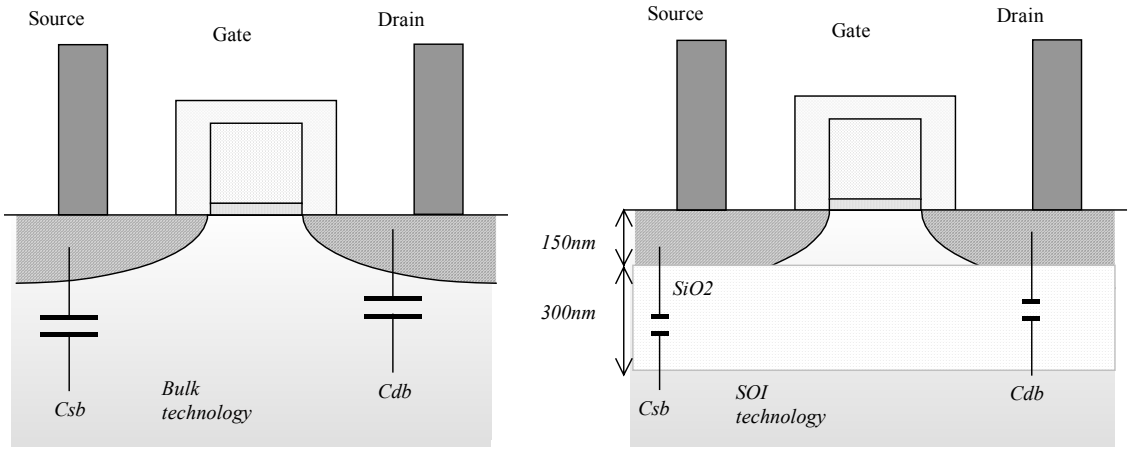
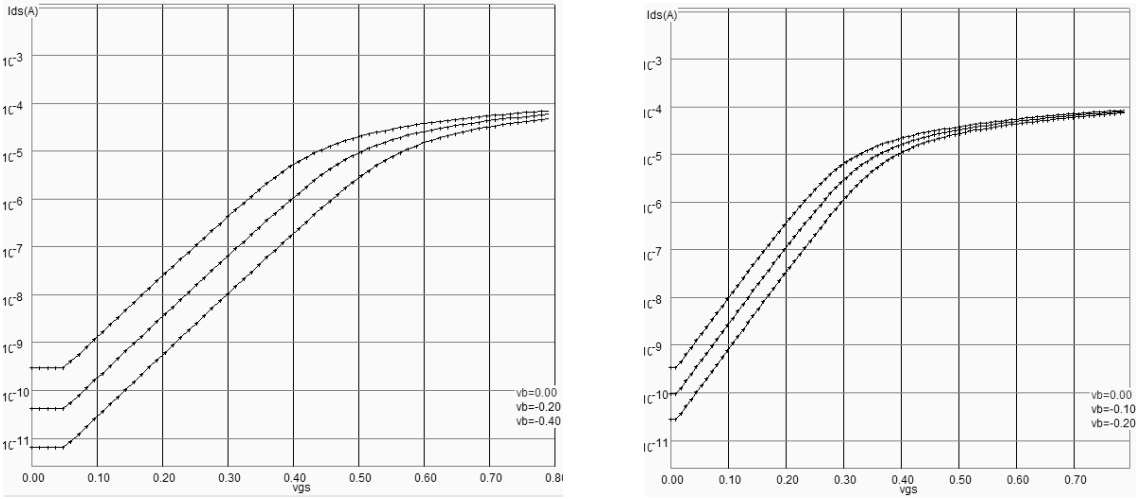


Figure 15-xxx: The junction capacitance between the source and bulk is almost eliminated in the case of SOI.

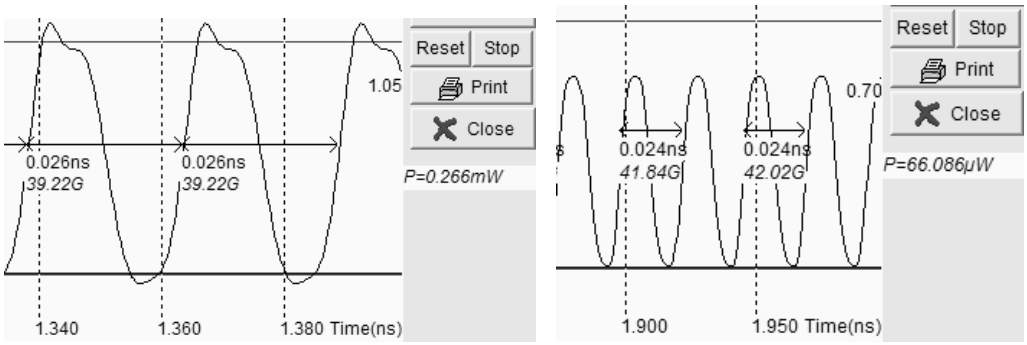
Low voltage Operation

An important feature of SOI devices is the steeper sub threshold slope due to a reduction of the substrate body effect. Typical sub threshold slope factors (NFACT in the BSIM4 menu) are close to 1.0 for SOI devices, as compared to 1.5 for bulk devices. For a given Ioff current, the SOI circuit may have a much smaller threshold voltage, which means that the circuit can operate at lower supply.



(a) Bulk MOS *(b) SOI MOS*

Figure 15-xxx: The steeper sub-threshold slope enables low voltage and low power operations.



(a) Bulk oscillator at 40GHz: 266µW *(b) SOI oscillator at 40GHz: 66µW*

Figure 15-xxx: The lower Ioff current and steeper sub-threshold slope enables low voltage and low power operations.

Recall that the power is proportional to the total circuit capacitor and the square of the supply voltage. This means that SOI circuits are very good candidates for low power operations as the parasitic capacitance is reduced and the supply voltage can be lowered. Considering the ring oscillator with three inverters, we obtain a 42GHz oscillation at a supply voltage of 0.7V in SOI technology, rather than 1.2V in bulk technology. The power gain is approaching a factor of 4.

Also, the lower sub threshold combined with a stepper slope is of key interest for analog circuits, which can provide the same functionality, with the same performances, with a lower power consumption.

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Increased density

One important feature of the SOI technology concerns the CMOS cell density increase thanks to relaxed design rule constraints between N+ and P+ diffusions. In CMOS bulk technology, the n-channel device is separated from the p-channel device with at least 12 lambda. In SOI technology, the design rule drops to only 2 lambda, as shown in figure 15-xxx.

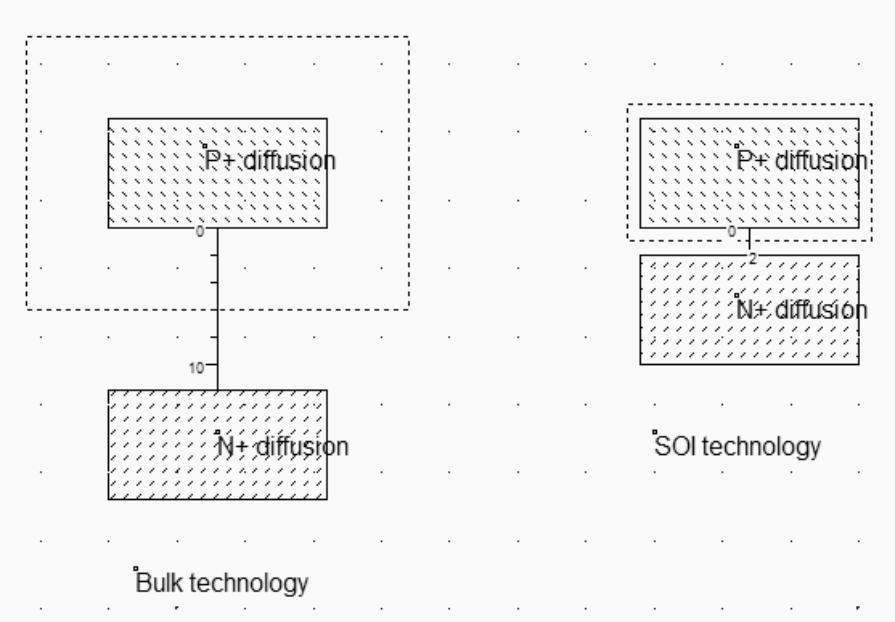


Figure 15-xxx: The increased density due to relaxed design rules between N+ and P+ diffusions (SOIDiffusion.MSK)

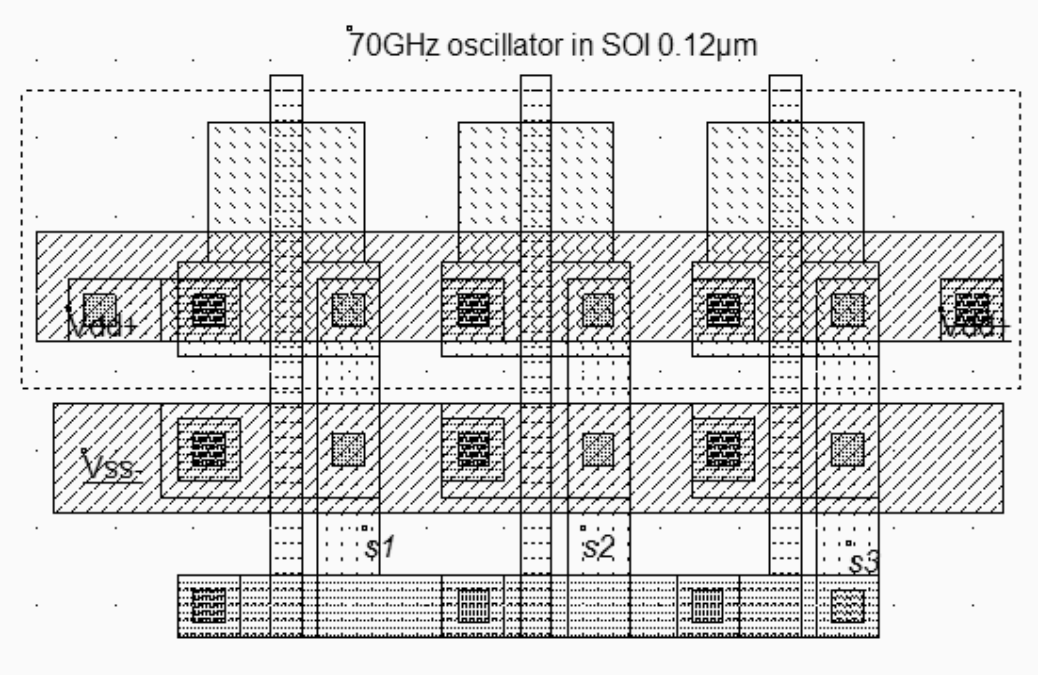
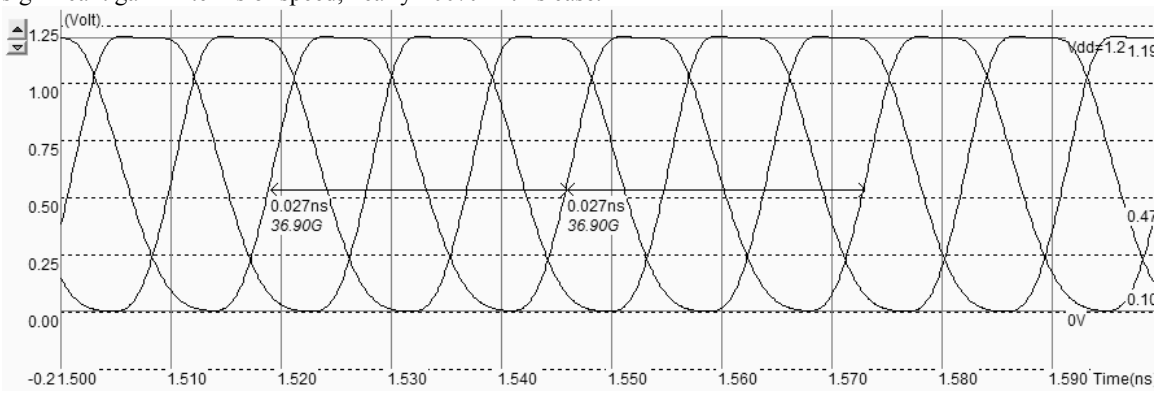


Figure 15-xxx: The ring oscillator in SOI technology (Inv3SOI.MSK)

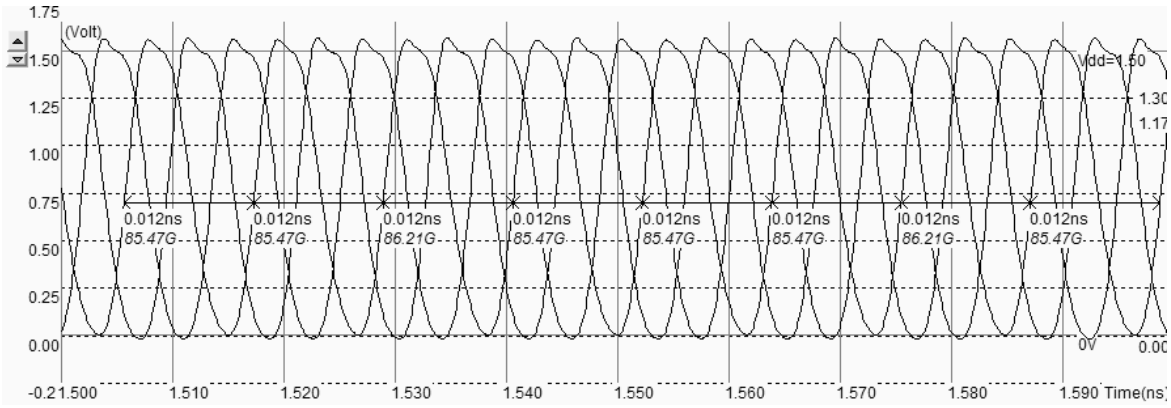
Consequently, the layout implementation of a CMOS cell is more compact as the nMOS and pMOS devices almost touch each other. As an example, the 3-inverter ring oscillator in SOI technology is 20% more compact that the bulk version.

Increased Operating Frequency

The comparison between the SOI ring inverter and the bulk ring inverter is given in figure 15-xxx. We observe a very significant gain in terms of speed, nearly 100% in this case.



(a) Bulk technology



(b) SOI technology

Figure 15-xxx: The simulation of the ring oscillator in bulk and SOI technologies (Inv3.MSK, Inv3SOI.MSK)

The very important frequency increase observed in figure 15-xxx mainly finds its origin in the decreased parasitic capacitance of the drain junctions of the MOS devices. As no long interconnect was needed in this design, the reduction of capacitance has a very clear impact on the final frequency. Furthermore, the maximum current available with the SOI MOS is 20% higher than for the bulk version, due to a particular undesired effect (The kink effect) described in the next section.

Decreased couplings

The oxide isolation has a positive impact on the noise immunity between blocks. One of the main contributors to noise is the substrate in bulk technologies. A high power, high frequency circuit such as a power amplifier may inject a fraction of its switched energy to the substrate that may be injected to sensitive parts such as input amplifiers or analog to digital converters. The insulator provided in the SOI technology has very efficient decoupling capabilities which facilitate the embedding of incompatible functionalities within the same silicon substrate

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Figure 15-xxx: Increased decoupling between noisy and sensitive circuits thanks to the insultaor

High Temperature Leakage

The Ioff current, corresponding to a zero gate voltage, determines the parasitic leakage current of the MOS device. A low leakage is important for low power operation. The behavior of SOI devices is better than the bulk device in terms of Ioff current at high temperature.

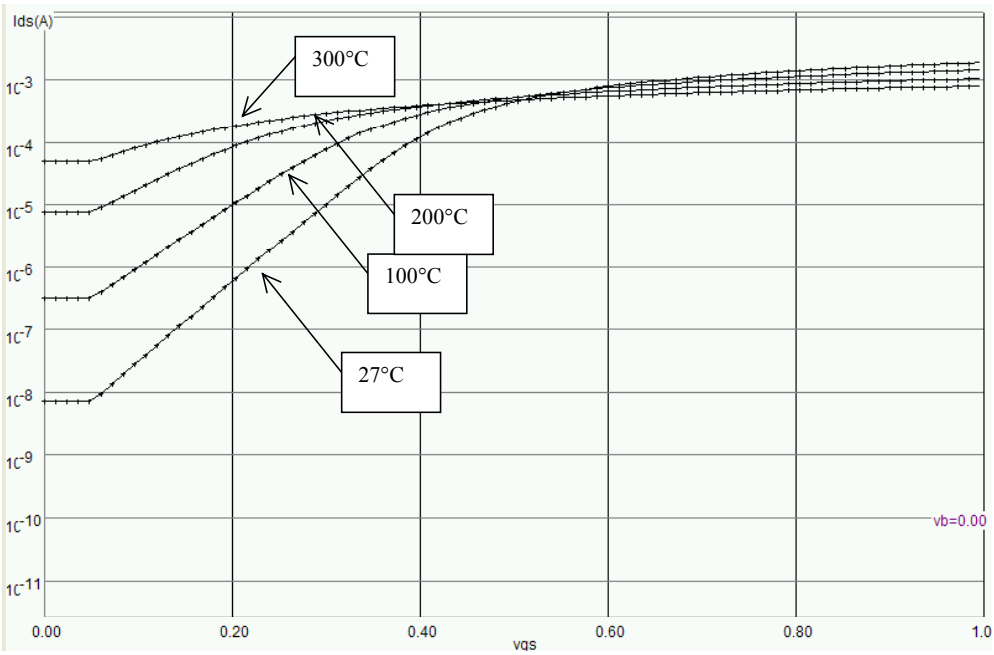


Figure 15-xxx: Temperature effects in bulk MOS devices (Low leakage W=10µm, L=0.12µm)

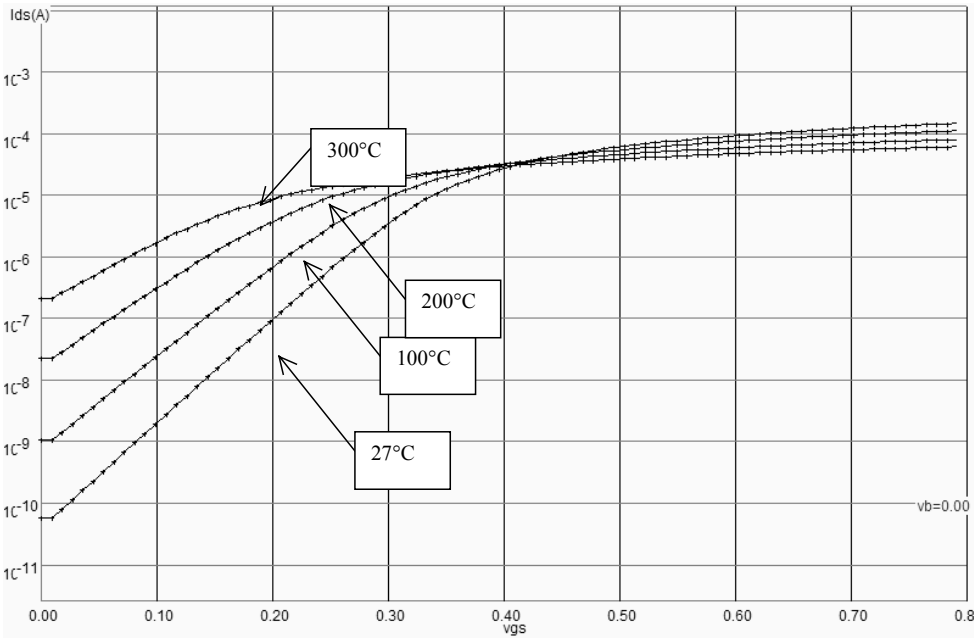


Figure 15-xxx: Temperature effects in SOI MOS devices (Low leakage W=10µm, L=0.12µm)

[Kuo p189]

2. SOI technology issues

Kink effect

In SOI technology, when a n-channel MOS transistor passes strong current between the drain and the source, a parasitic phenomenon called Kink effect appears [Kuo p52]. The current Ids suddenly rises and provokes a conductance discontinuity, usually between 0.5V and 1V in 0.12µm CMOS process. The origin of this parasitic effect is the impact ionization of high energy electrons entering the drain region, which create supplementary positive and negative charges below the gate. While electrons participate to the Ids current, the underlying insulator prevents the positive charge from being evacuated to the substrate, as it would happen in bulk technology thanks to the natural ground connection of the substrate. In the case of SOI, the body of the MOS device may rise significantly, without any direct control. The rise of the local voltage below the gate has an instant impact on the threshold voltage which is lowered.

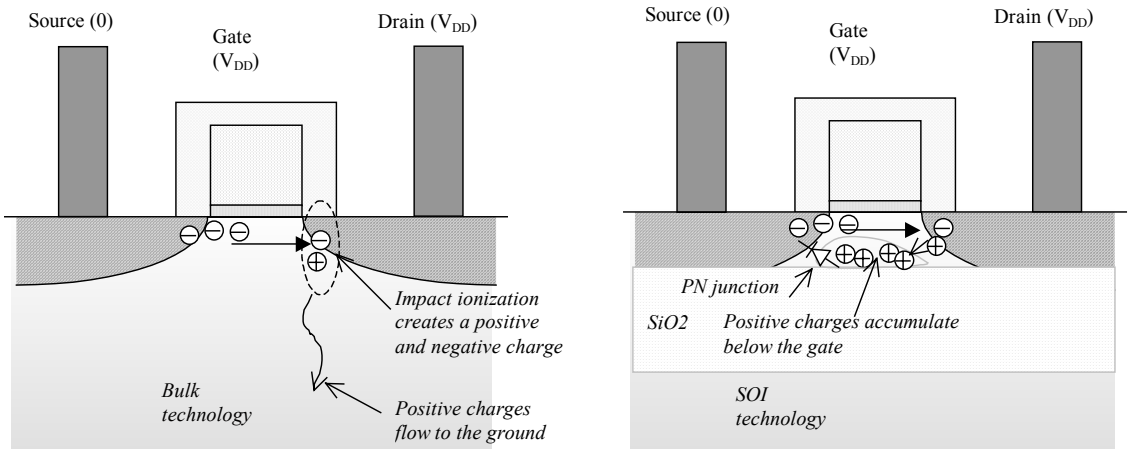
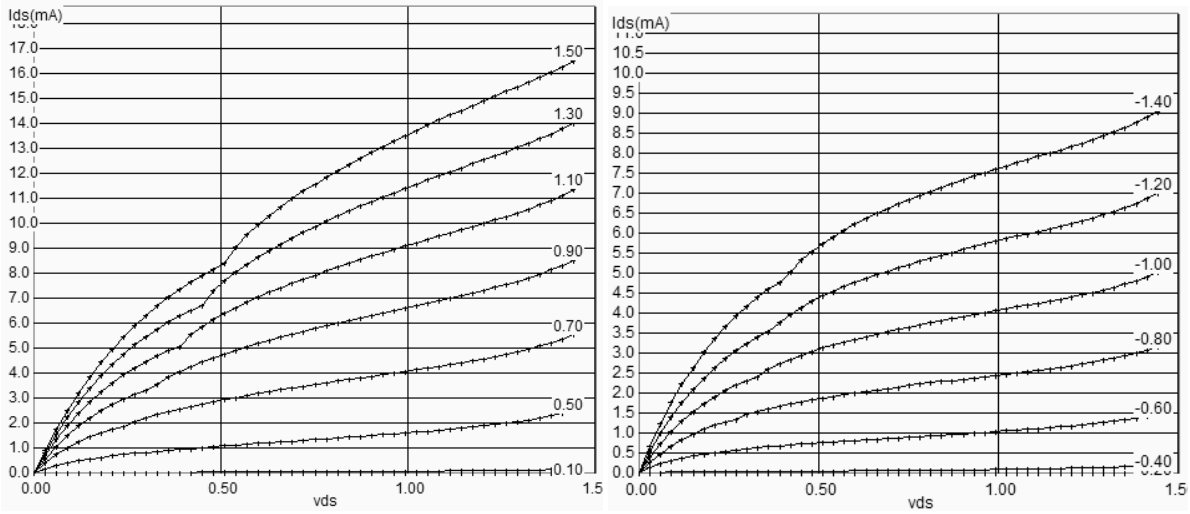


Figure 15-xxx: The impact ionization creates an accumulation of positive charges below the gate in the case of SOI



(a) n-channel MOS *(b) p-channel MOS*

Figure 15-xxx: The drain current characteristics of the n-channel and p-channel SOI devices show a kink effect near saturation

At a certain point, the bias of the PN junction between the P-doped bulk and the N+ source diffusion is high enough to turn on the junction, which leads to a sudden channel current increase, as seen in the characteristics (Figure 15-xxx). This effect is also called floating body effect (FBE). The impact ionization is more severe in the case of n-channel MOS devices than for p-channel MOS devices. In the characteristics of figure 15-xxx, the kink effect is more pronounced for the n-channel than for the p-channel.

Fully Depleted MOS

A possibility for reducing the floating bulk effect is to use a very thin diffusion for the channel, so that there is no more room for accumulation of positive charges, and consequently almost no kink effect. The source and drain diffusions are usually manufactured with an increased thickness on the top of the SiO2 insulator.

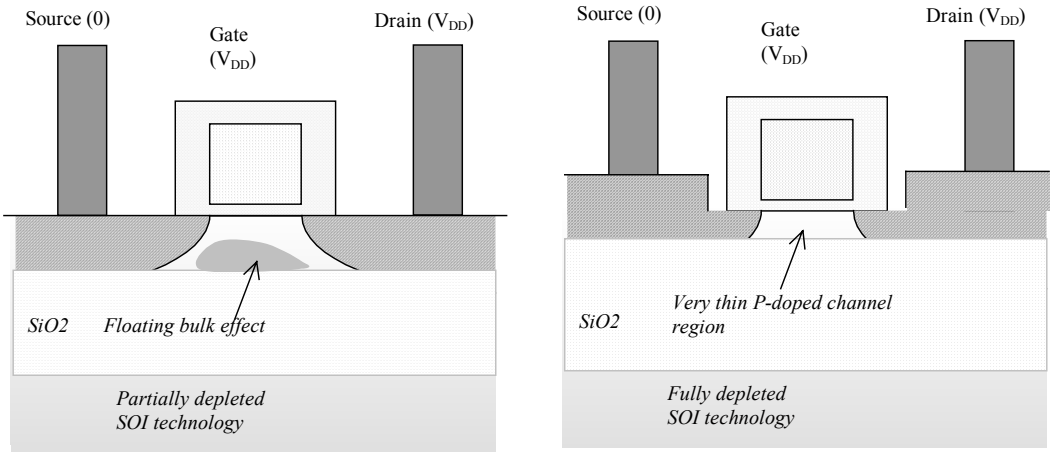


Figure 15-xxx: The fully depleted MOS device has no more Kink effect, but several manufacturing and design drawbacks

The fully depleted MOS devices are much harder to manufacture and control. The process-controlled threshold adjustment required for low-Vt, high speed and ultra-high speed MOS devices is very complex due to the very thin diffusion area below the gate. These drawbacks have made the fully depleted MOS less attractive than partially depleted MOS. The SOI process parameters provided in Microwind correspond to a partially depleted MOS technology.

3. SOI Device Model

Bulk silicon models such as LEVEL 3 or BSIM4 typically do not include source/bulk diode currents because the junctions are usually reverse-biased, and can be considered as junction capacitors. This is not the case for SOI devices where the source/bulk junctions can be significantly forward-biased due to the impact ionization which provokes the accumulation of positive charges below the gate.

Fully depleted MOS model

The kink effect is very weak in fully depleted SOI MOS devices. Consequently, the BSIM4 model may be applied with reasonable accuracy as the underlying physics and working principles are similar.

Partially depleted MOS model

In Microwind, the kink effect is modelized in the case of partially depleted SOI devices, thanks to a new parameter. Details on the SOI model in SPICE are provided in chapter 7 of [Kuo], considering the lateral bipolar device made of the source, the channel and the drain regions (NPN structure in the case of an N-channel device). A more simple implementation proposed in Microwind consists in modifying directly the saturation current model, where the Kink effect is the most important. The BSIM4 main current model is given in equation 15-xxx.

The new parameter is introduced, called Asoi. The kink effect occurs when Vds is higher than the saturation voltage Vdsat. The parameter Asoi determines the amplitude of the kink. A new term is introduced, as shown in equation 15-xxx. This approach is a simplified version of the model used in BSIM3 SOI device model [Berkeley].

$$Ids = I_{ds\_bsim4}(1 + \frac{\text{ASOI}}{L_{eff}.Vt.\sqrt{V_{DS} - V_{dsat}}})$$

L = device channel length (m).

Vds= voltage difference between drain and source (V)

Vdsat= saturation voltage as defined in equation 3-xxx (V)

Vt = threshold voltage of the MOS device (V)

Asoi = technological parameter for handling the kink effect (default 2e6 V/cm)

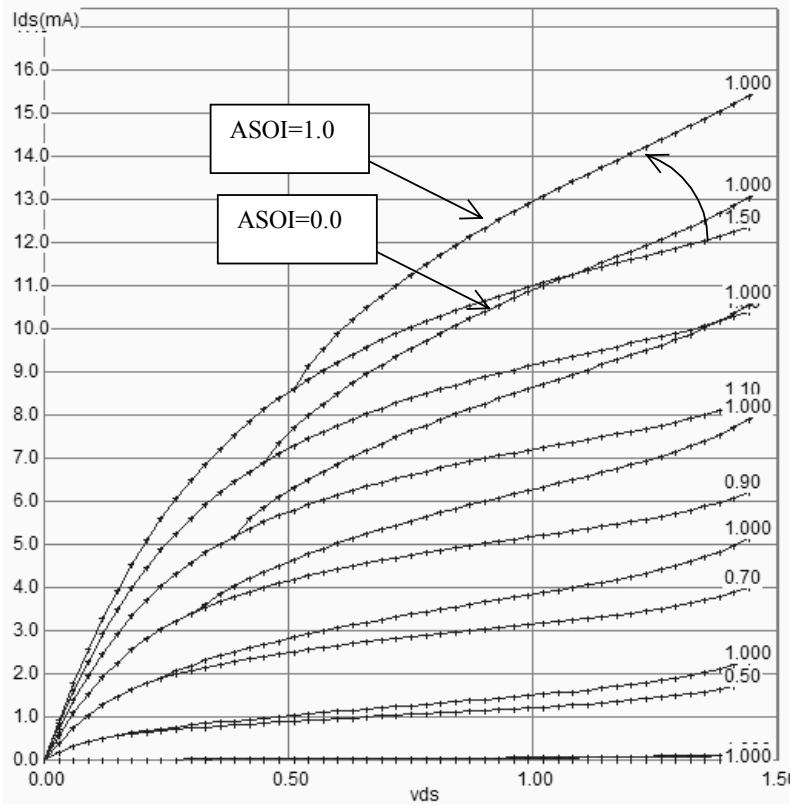


Figure 15-xxx: The effect of the ASOI parameter on the Id/Vd characteristics (Using soi012.RUL)

As the oxide thickness scales down to 2nm and below, the quantum mechanism of direct tunneling through the gate oxide rises exponentially. The gate current becomes large enough to compete with the channel current and consequently affect the body potential. Much more complex models such as BSIMPD [BsimPd] have been developed for an accurate simulation of these nano-scale MOS devices.

Temperature dependence

[Kuo p189]

4. SOI Design

Floating Body Device

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Body grounded Device

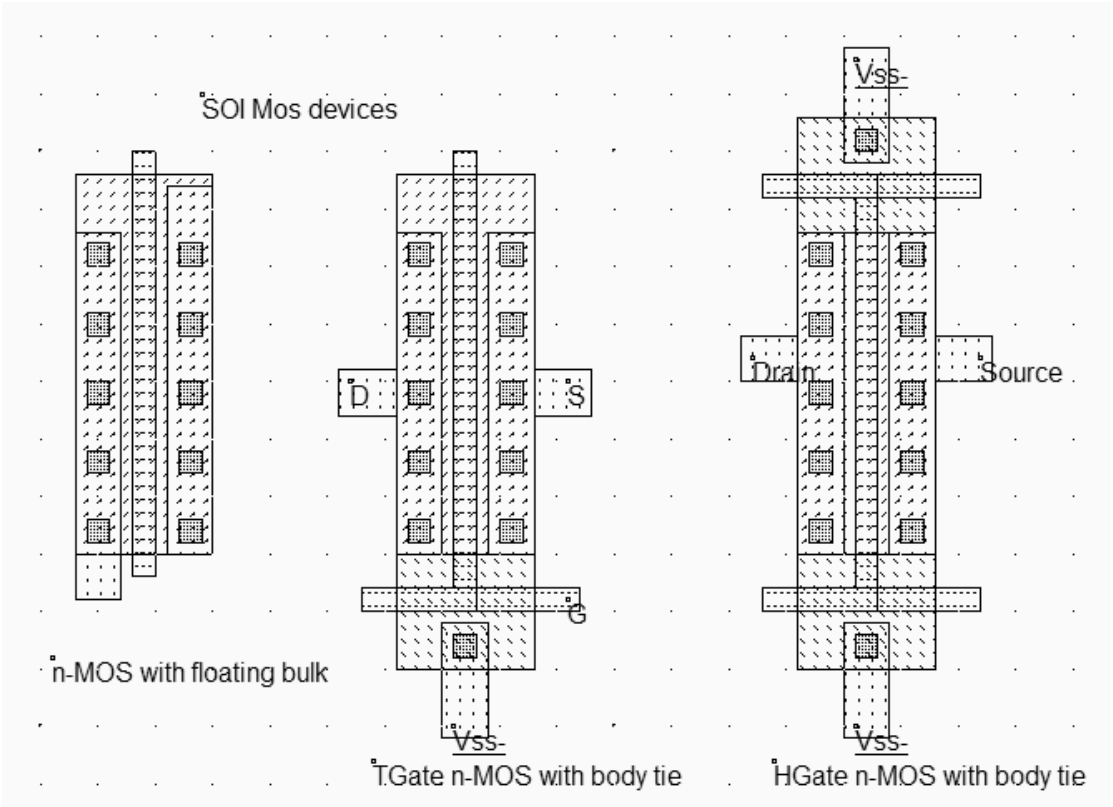

Figure 15-xxx: Adding a contact in partially depleted MOS to avoid the kink effect (mosSoi.MSK)

5. Future of SOI

Floating Body Device

The behavior of an SOI device depends on the thickness of the silicon layer. If the silicon layer is thick compared to the channel length, Because of this floating body effect (FBE), fabs cannot implement existing circuit designs in partially depleted SOI. To eliminate FBE, the design could introduce an additional ground contact, but that takes up valuable circuit space. Alternatively, design models can account for the FBE and work around it. According to Celler, only about 1 percent of the transistors in a typical circuit are unable to tolerate FBE and must be grounded.

impact ionization. This reaction of the bipolar transistor to current
passing through the nearby MOS transistor gives rise to a number of unwanted effects that complicate Silicon

SOI has been gaining momentum since 1998, when IBM announced it would use the material for its microprocessors. Still, skeptics, most notably Intel, questioned whether the performance gains of partially depleted SOI would scale. Last year at IEDM, Robert Chau and coworkers at Intel described their work with fully depleted SOI transistors. In fully depleted SOI, the silicon layer is much thinner – on the order of half the channel length. The depletion region near the gate oxide is on the same order as the silicon layer thickness. Fully depleted SOI eliminates the FBE, but the thinner silicon layer is much more difficult to manufacture.
As Hitachi's Digh Hisamoto explains, the source/drain contact resistance in fully depleted SOI is high because the thin silicon limits the depth of the source and drain. For that reason, Intel's SOI process includes elevated source and drain regions, constructed by selective epitaxy. Compared to bulk CMOS, Chau said, fully depleted SOI gives the same ratio between "on" current and "off" current, while reducing power consumption by 30 percent.

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the operation of the chip’s circuit and its modeling. Significant effort has been devoted in the last three decades in characterizing, modeling, eliminating or at least reducing, and controlling the unwanted effects caused by the bipolar device.
One solution to the bipolar transistor dilemma that has been under strong consideration over the last two-to-three years was to use very thin layer SOI films (less than 0.1 micron) called “fully-depleted films.” IBM’s approach has been different,

and it uses slightly thicker films (greater than 0.15 micron), called “partially-depleted films.”
Perhaps one of the biggest obstacles facing adoption of SOI as a mainstream technology has been steady progress in traditional bulk CMOS technology over the years. While much attention has been devoted to perfecting SOI, silicon bulk
technology has shown consistent advances.

But probably the single most important factor in SOI becoming a mainstream technology is the breadth and quality of work
done at IBM while developing it. The most important breakthrough, among many, was the recent demonstration of fully functional microprocessors and large static random access memory chips utilizing SOI. This work has convinced many skeptics that after three decades SOI is real technology that can be used to design the next generation of chips at profitable levels and achieve a two year performance gain over conventional bulk silicon technology.

Once the SOI film is made, the fabrication of the MOS devices and the metal interconnects is almost identical as for the bulk CMOS process.

At the same performance as bulk CMOS, IBM has proven that the chip power could be reduced by a factor of 2-3X [Ref IBM].

6. Conclusion

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Exercices

References

[Kuo] James B. Kuo, Shih Chia Lin "Low Voltage SOI CMOS VLSI Devices and Circuits", Wiley Intersciences, ISBN 0-471-41777-7, 2001
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